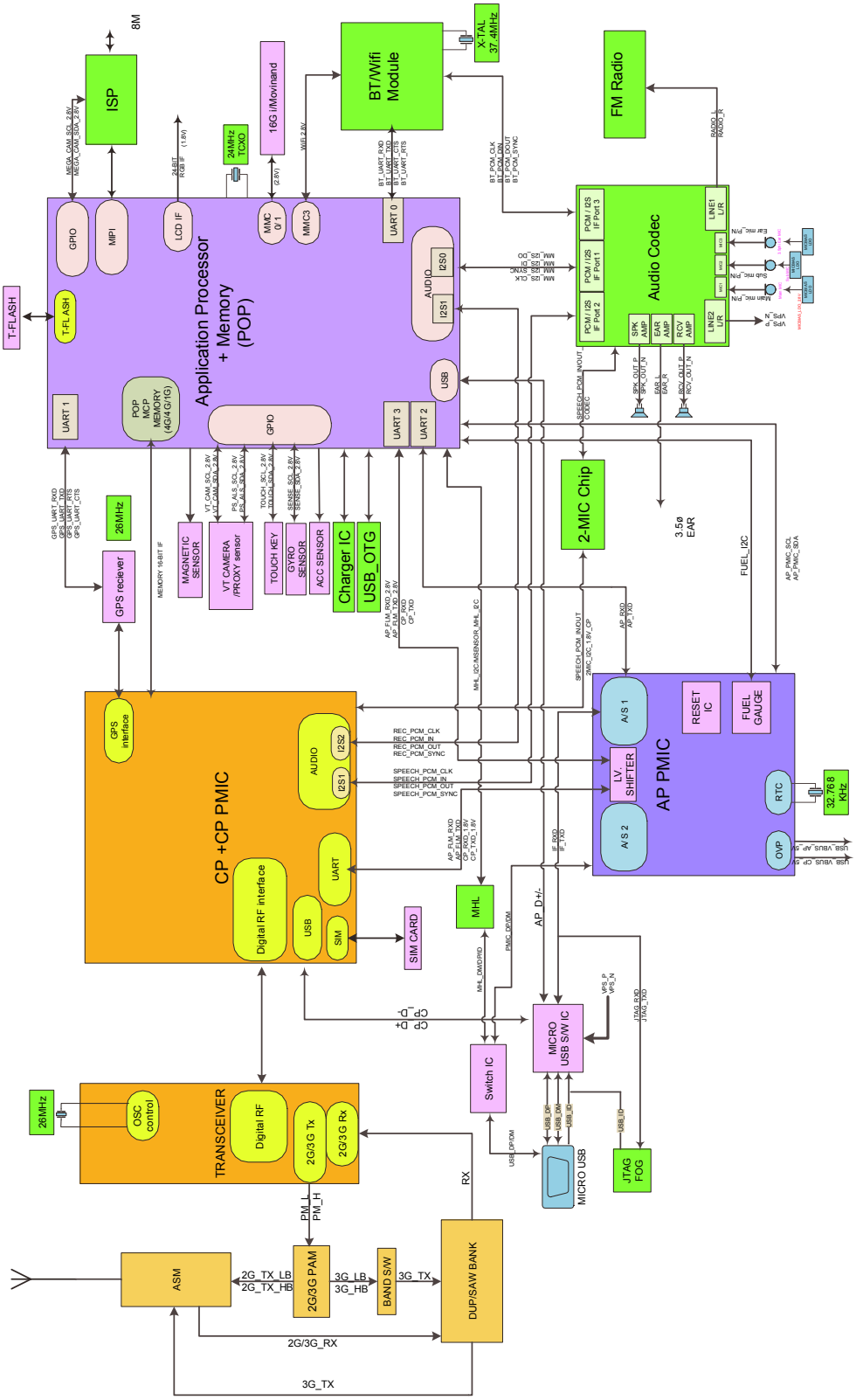
8. Level 3 Repair

8-1. Block Diagram



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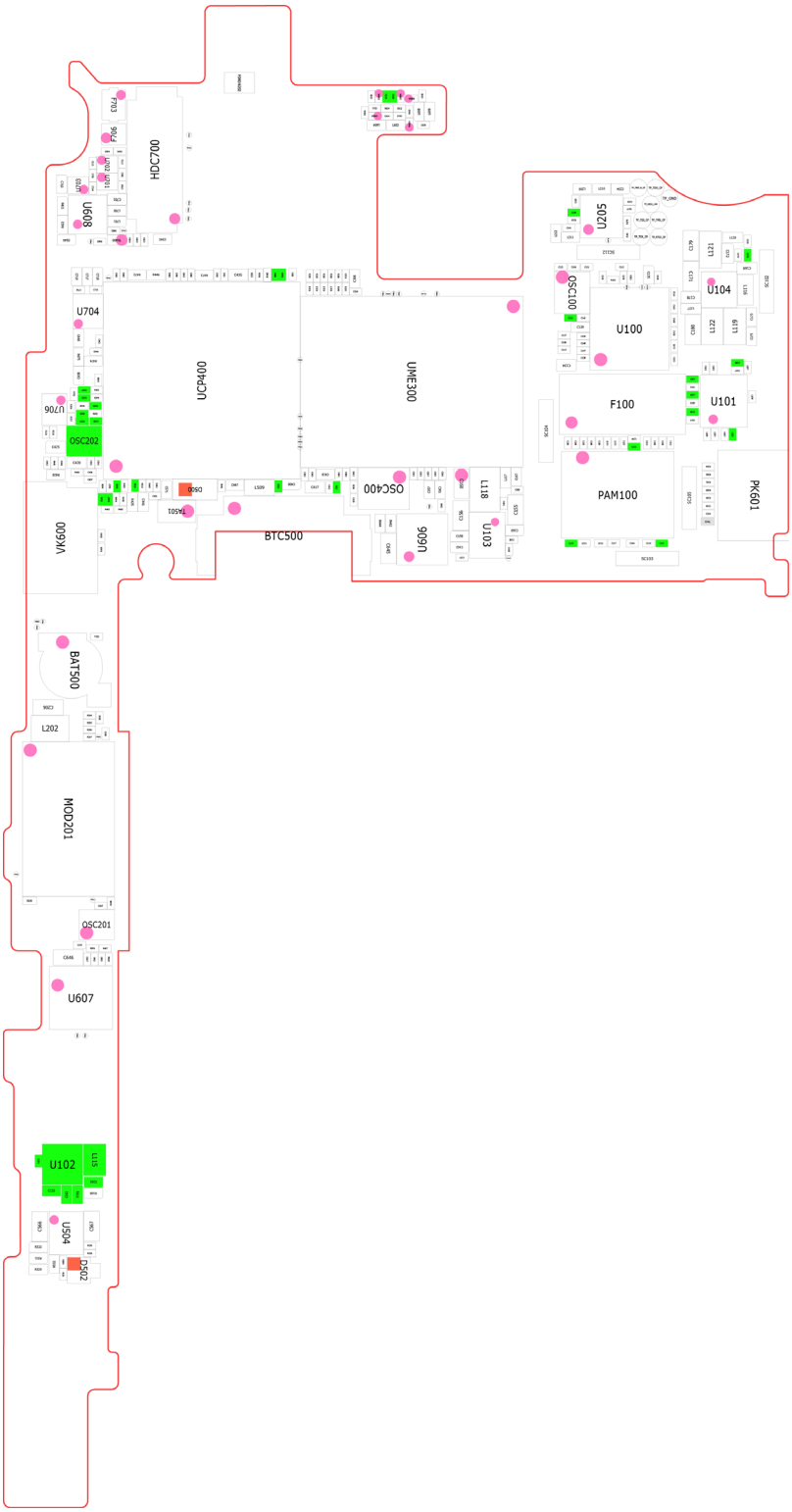
8-2. PCB Diagrams

8-2-1. Top



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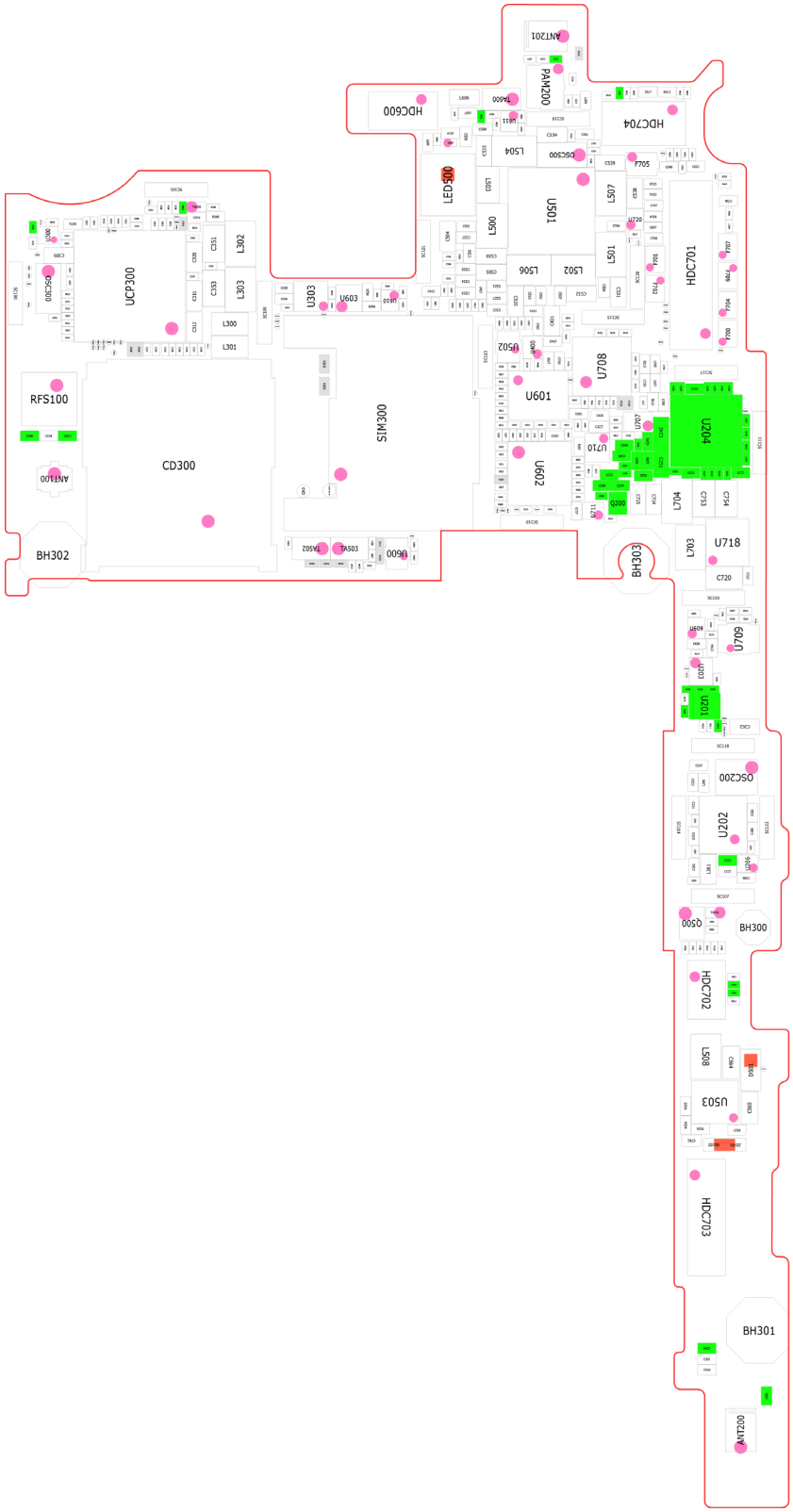
8-2-2. Bottom



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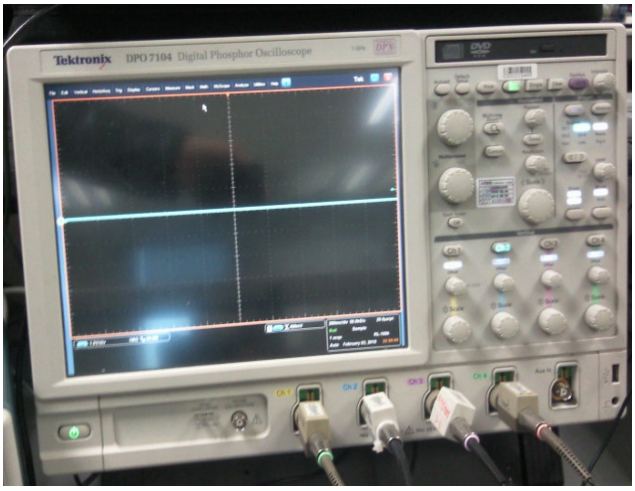
8-3. Flow Chart of Troubleshooting

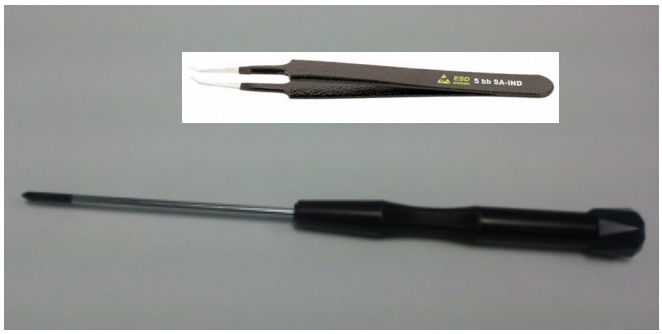
Equipments



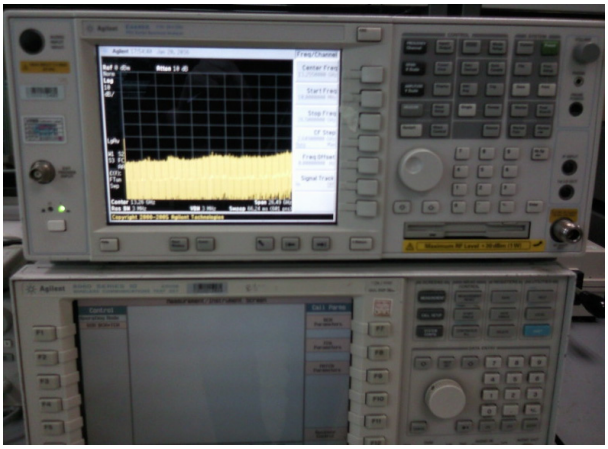
↑ Oscilloscope

á Digital Multimeter

á Power Supply



á + driver, ESD Safe Tweezer



↑ 8960 & Spectrum Analyzer

á Soldering iron

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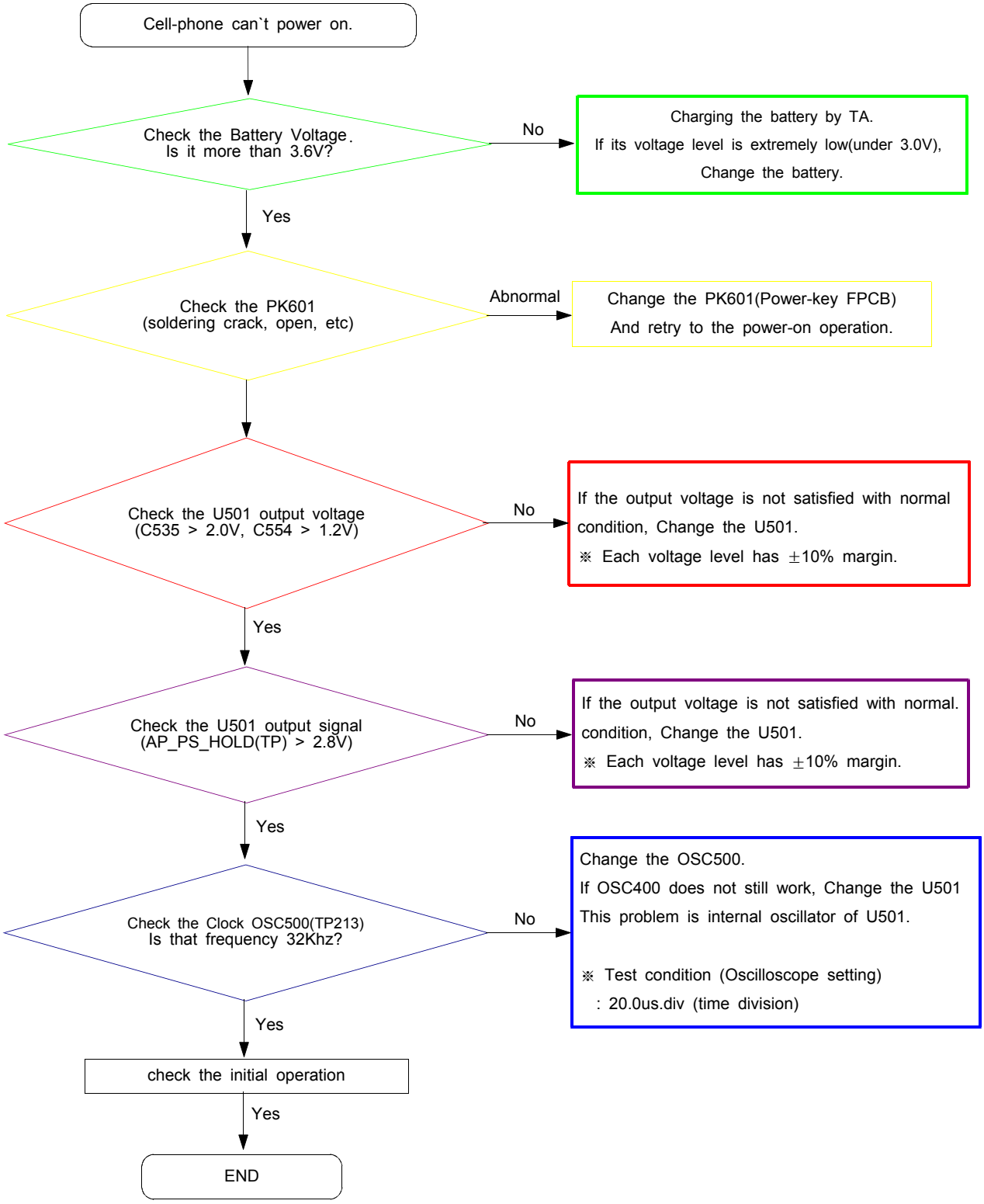
8-3-1. Power On



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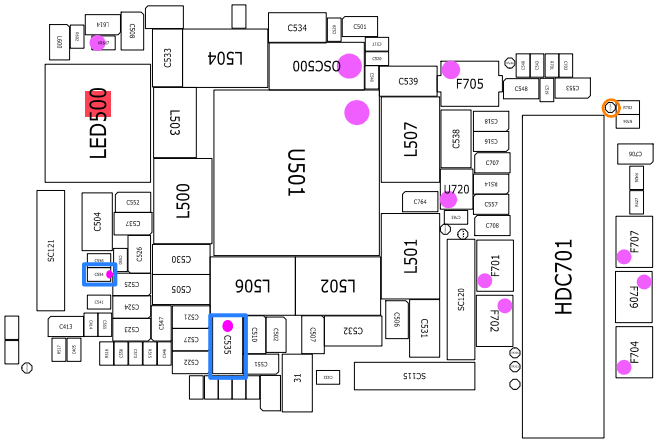

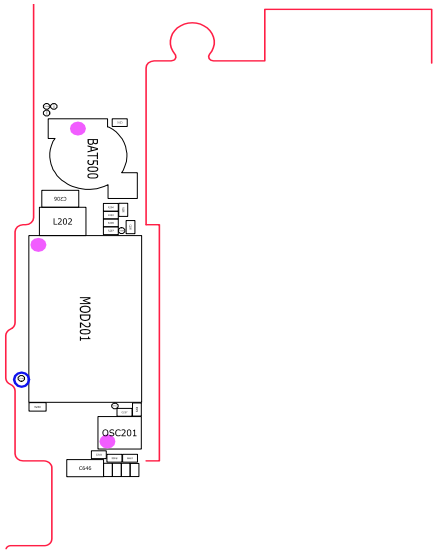

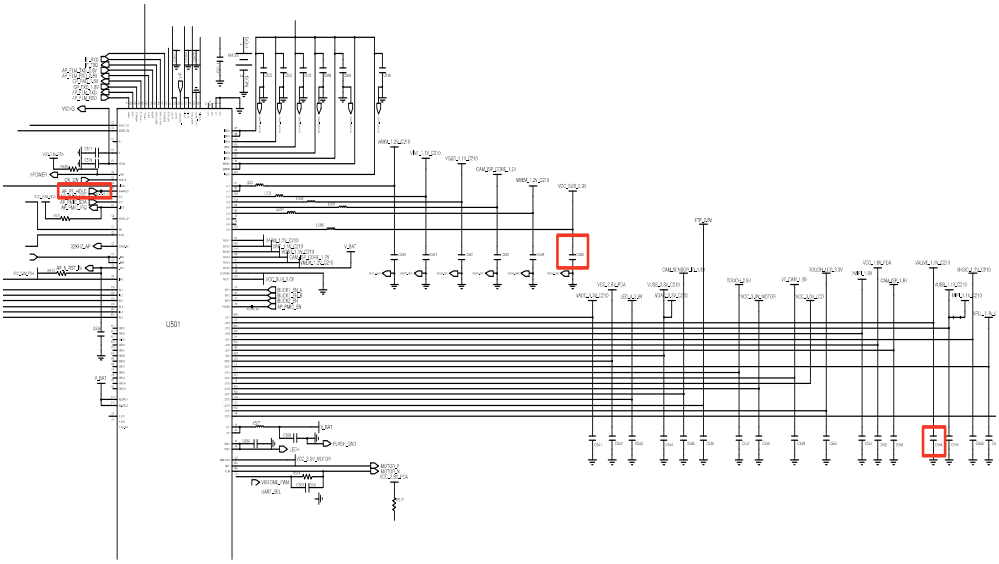

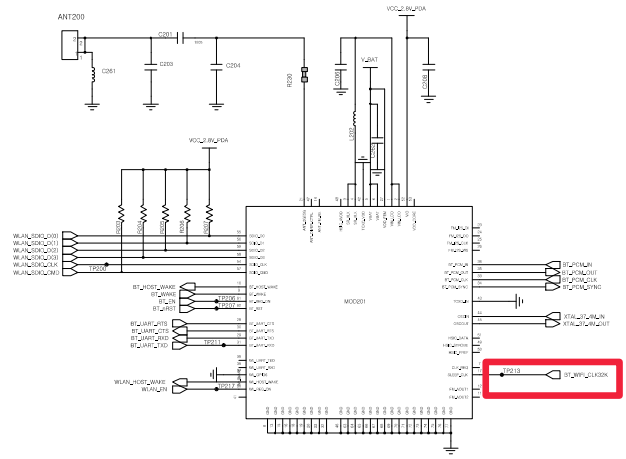

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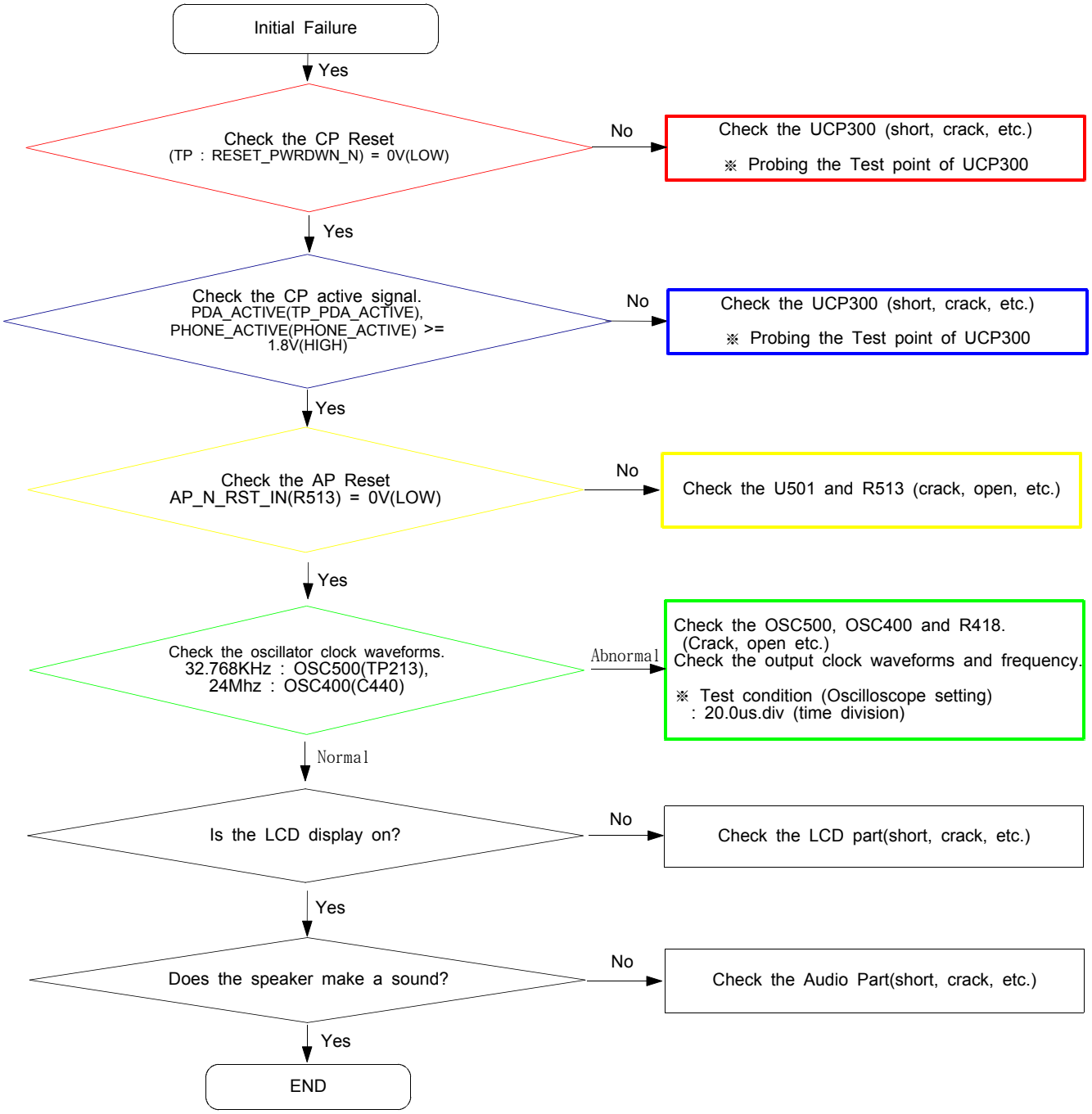
8-3-2. Initial



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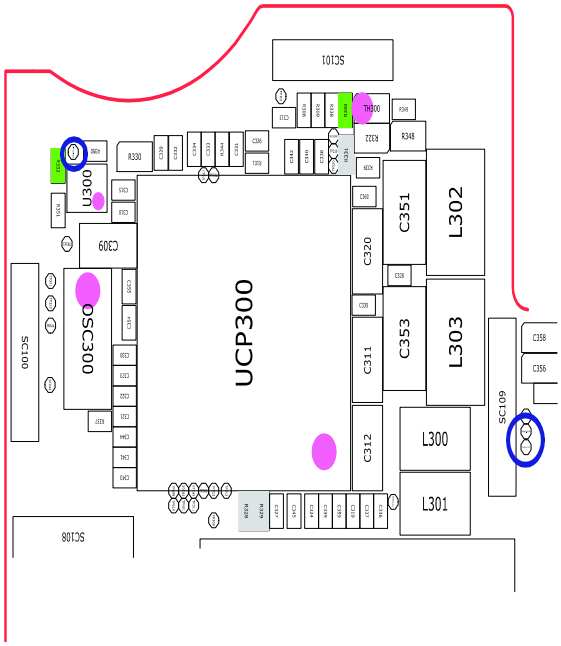

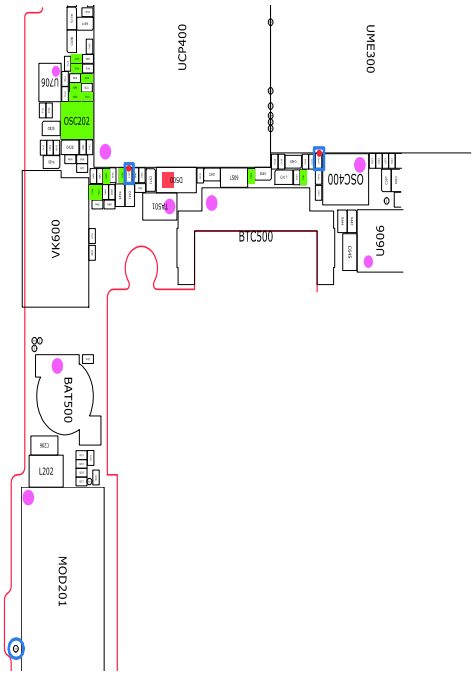

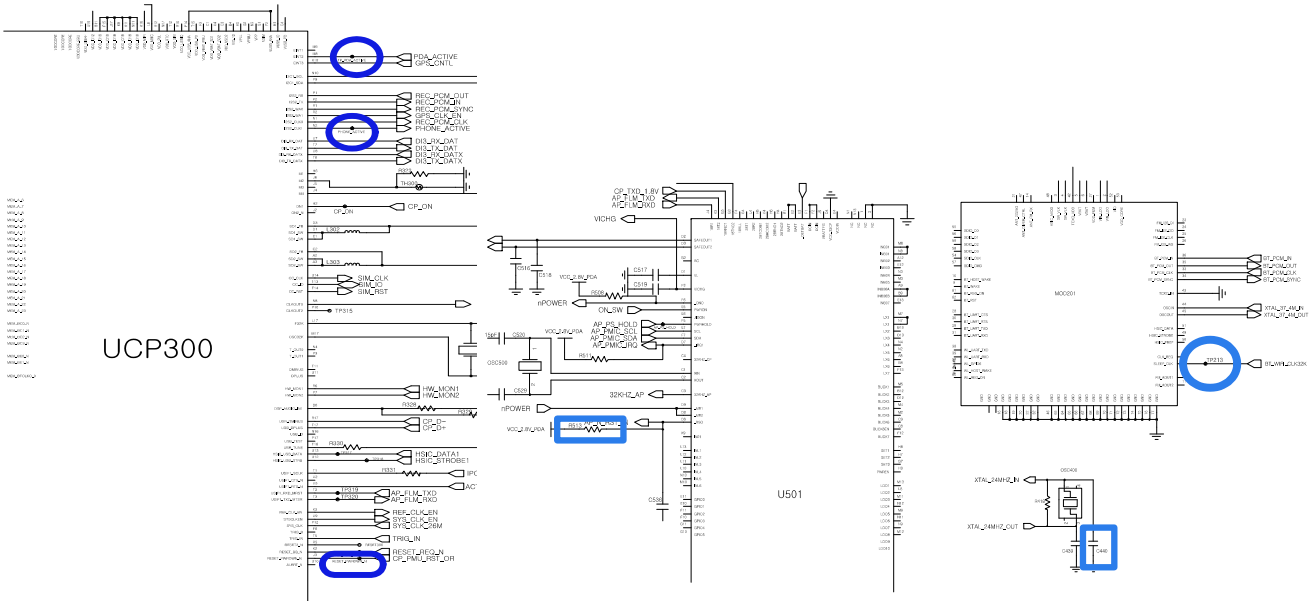

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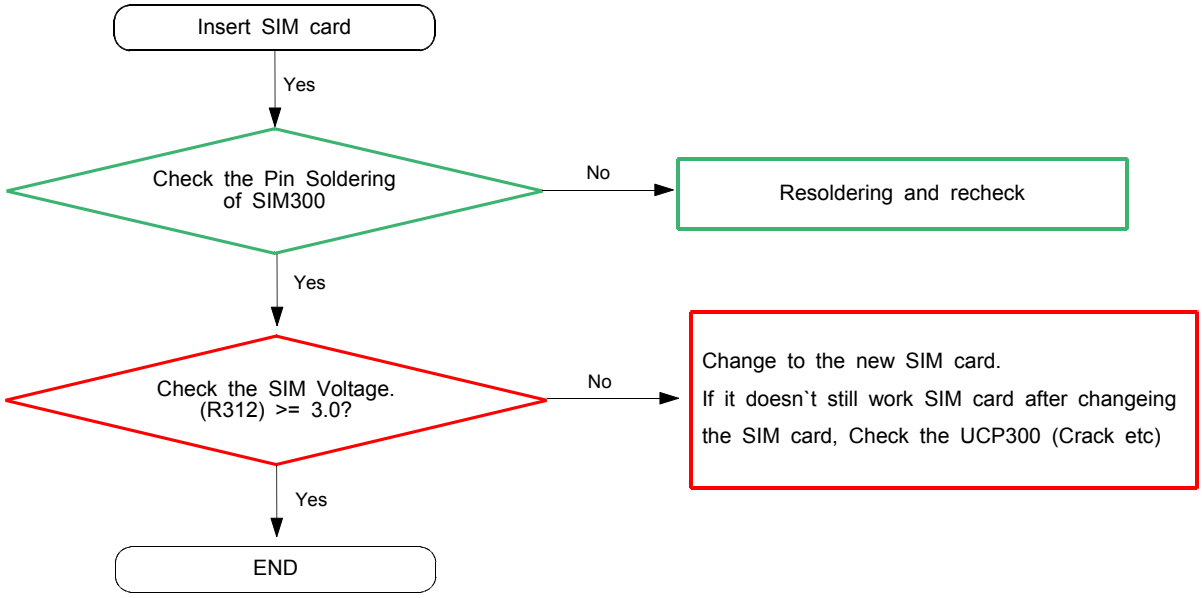
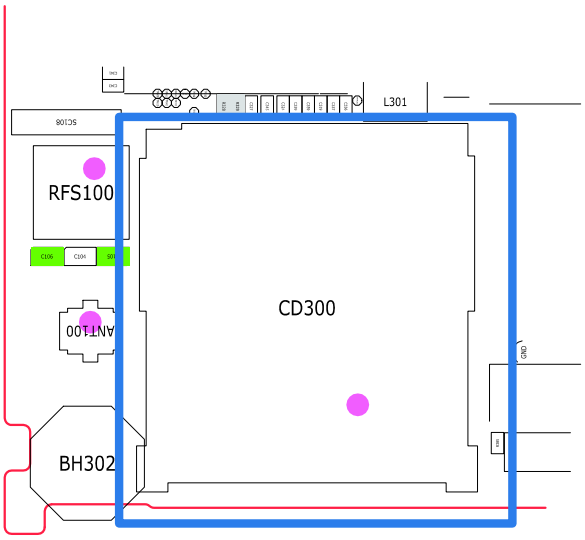
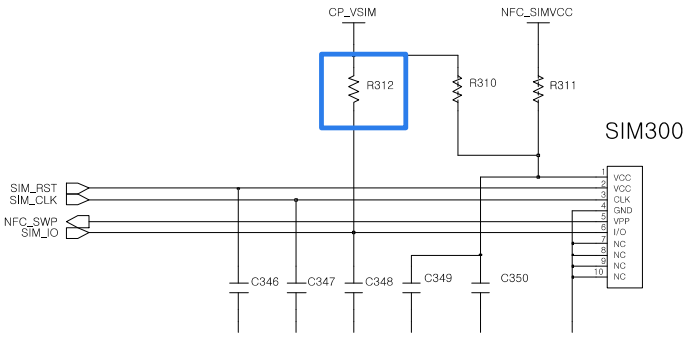
8-3-3. Sim Part







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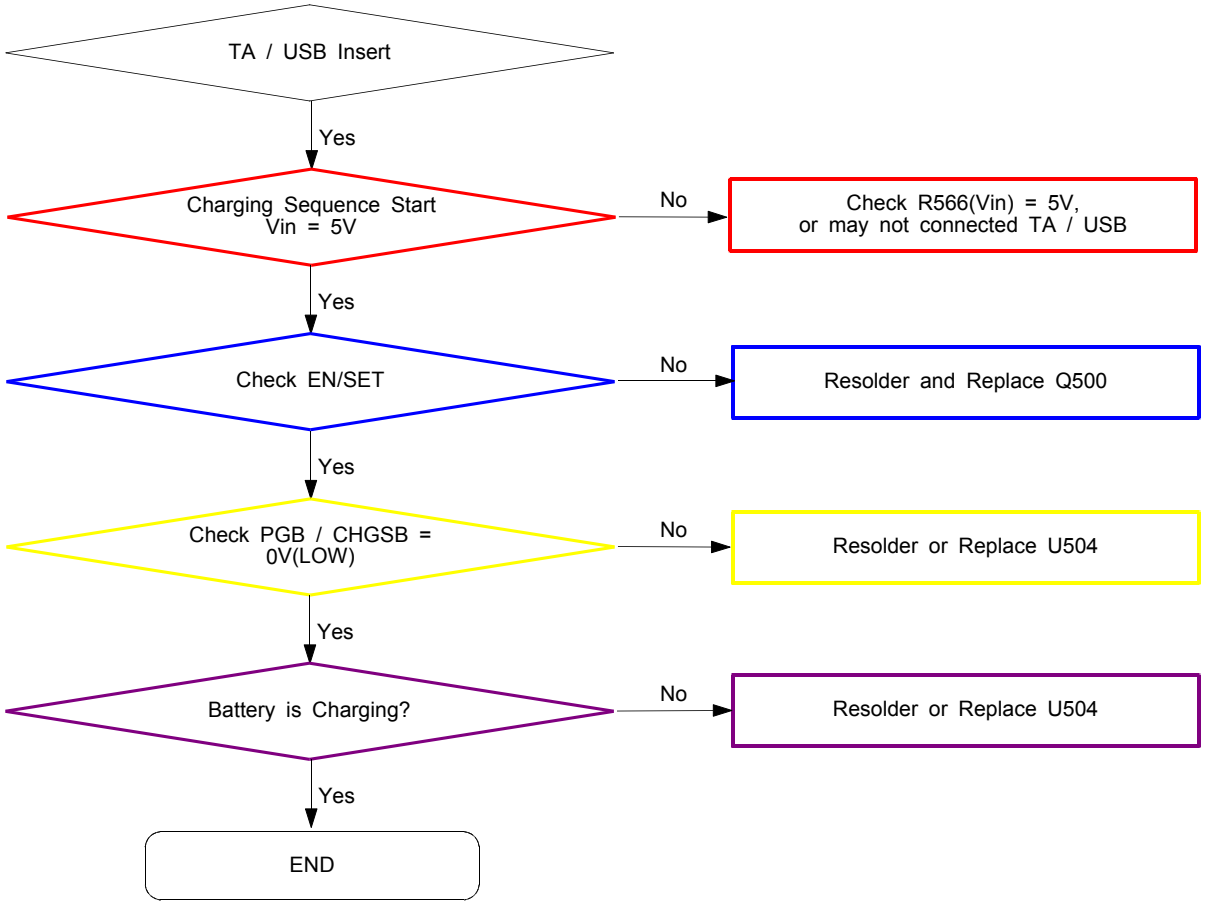

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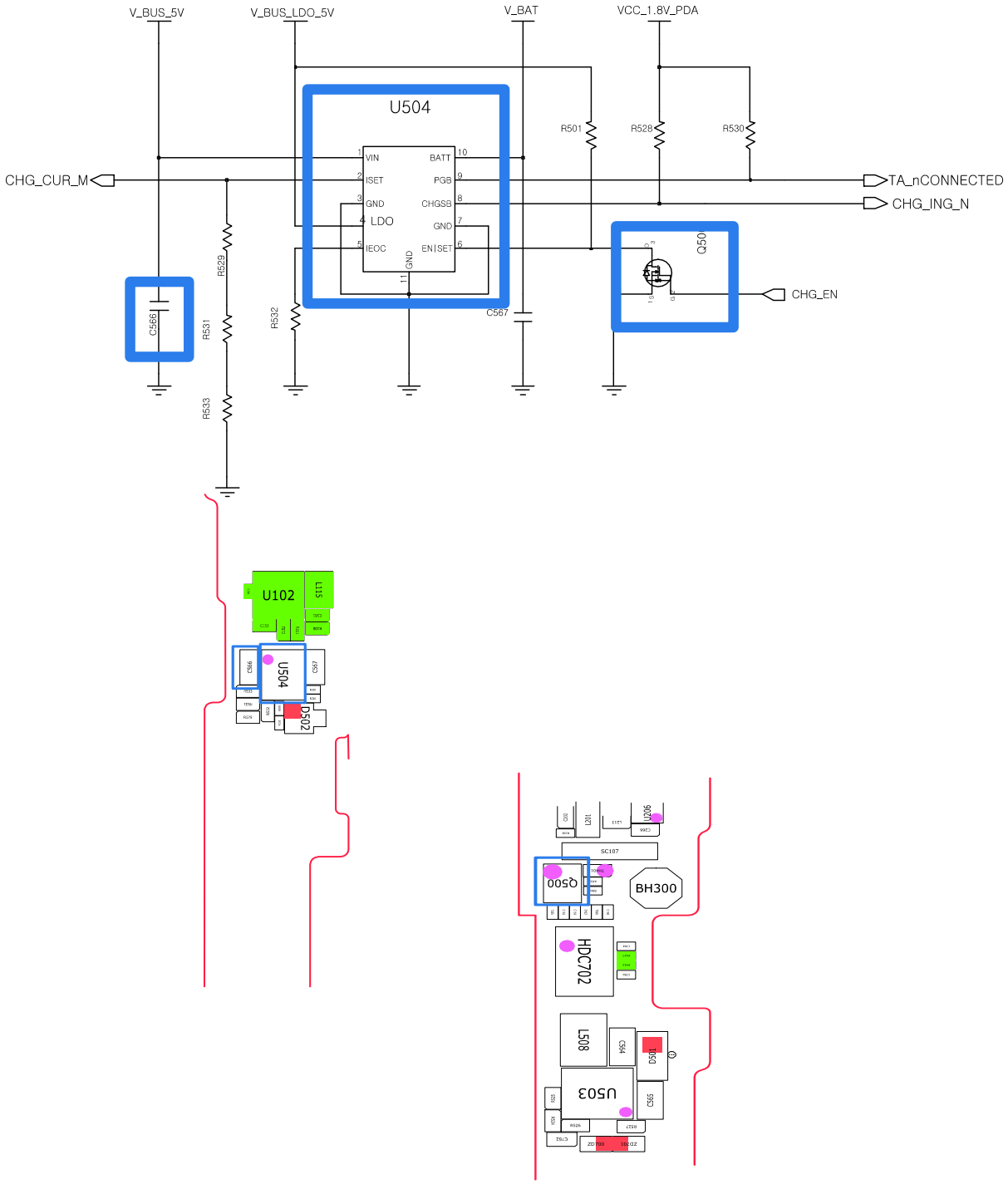

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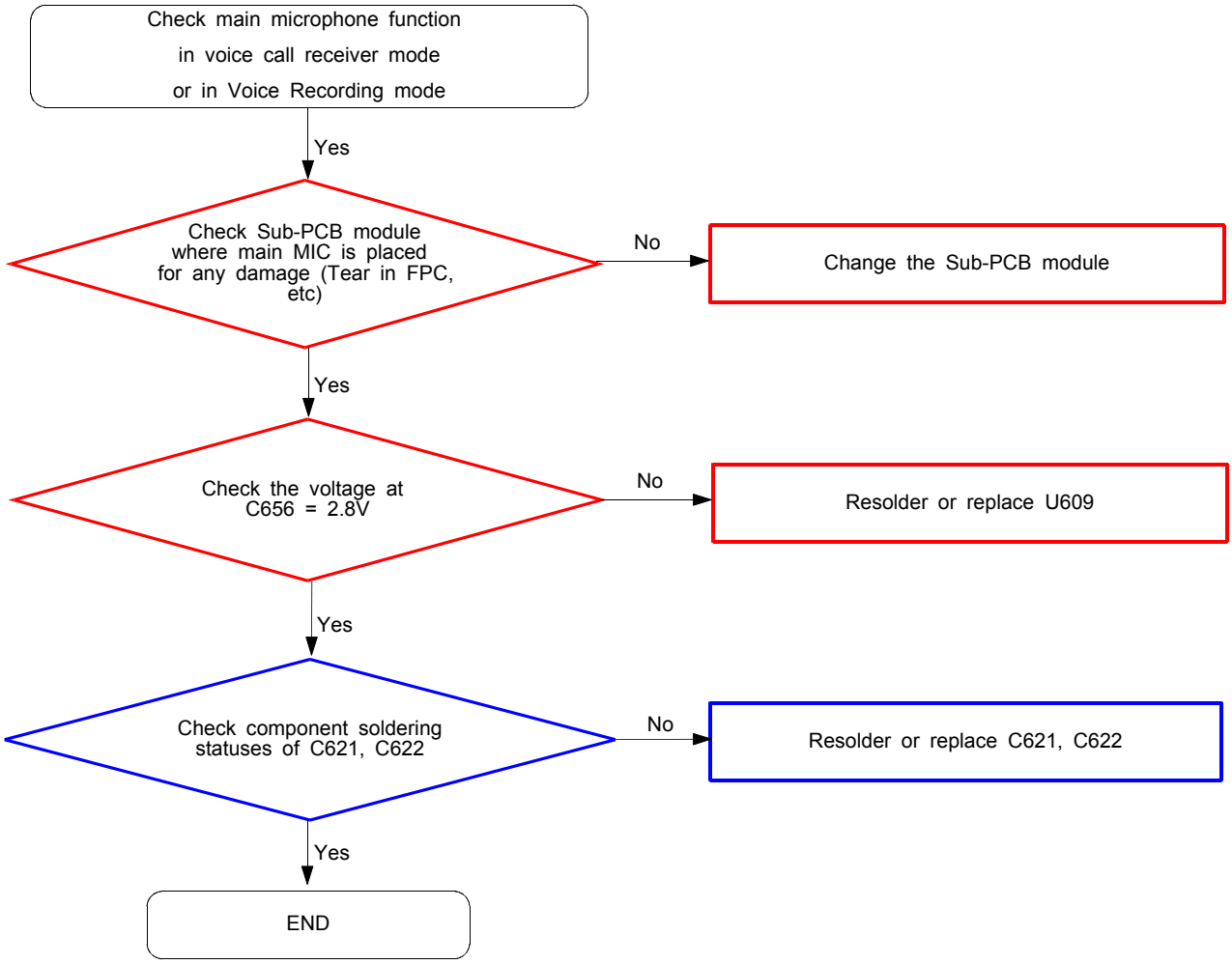
8-3-5. Microphone Part (Main MIC)



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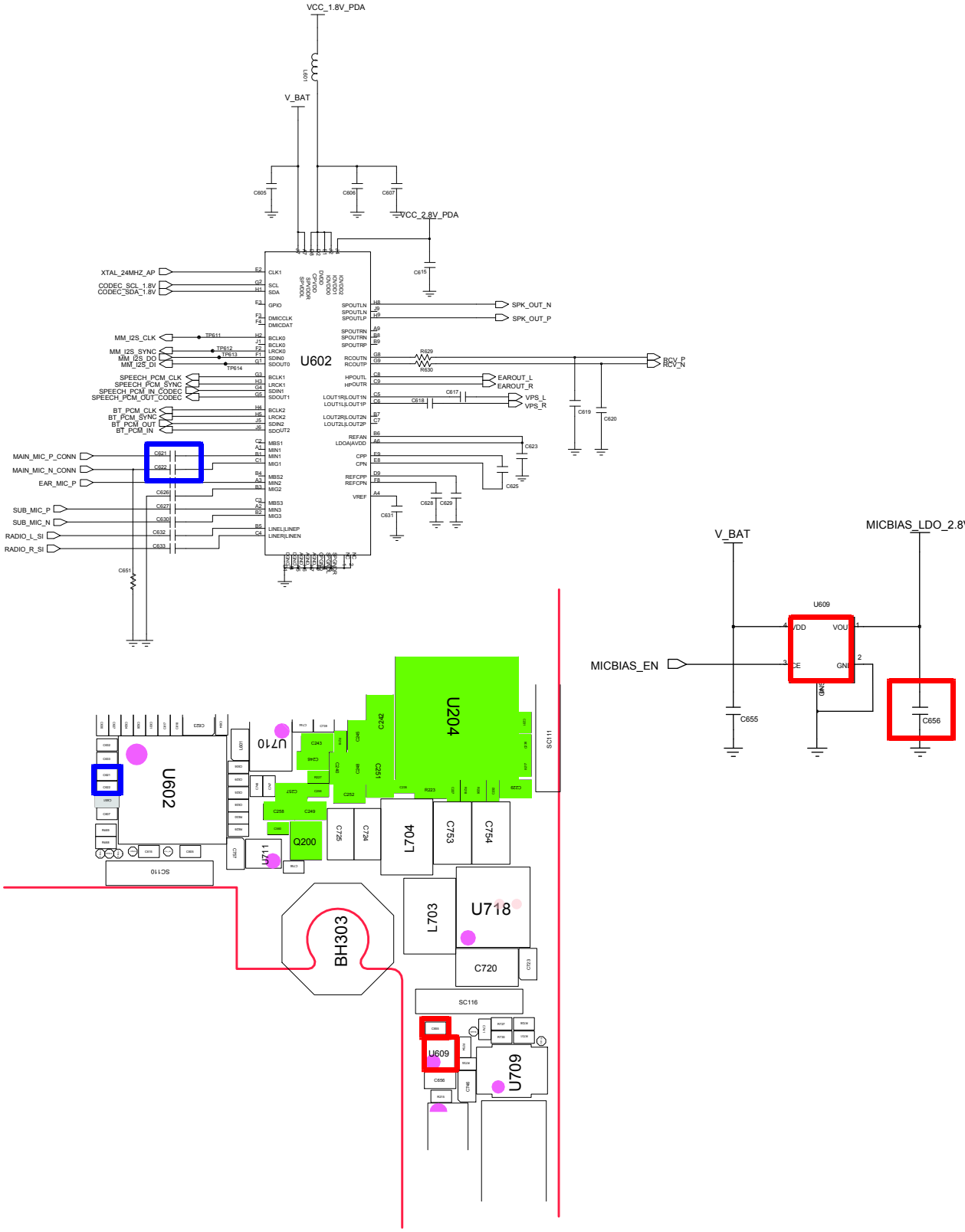

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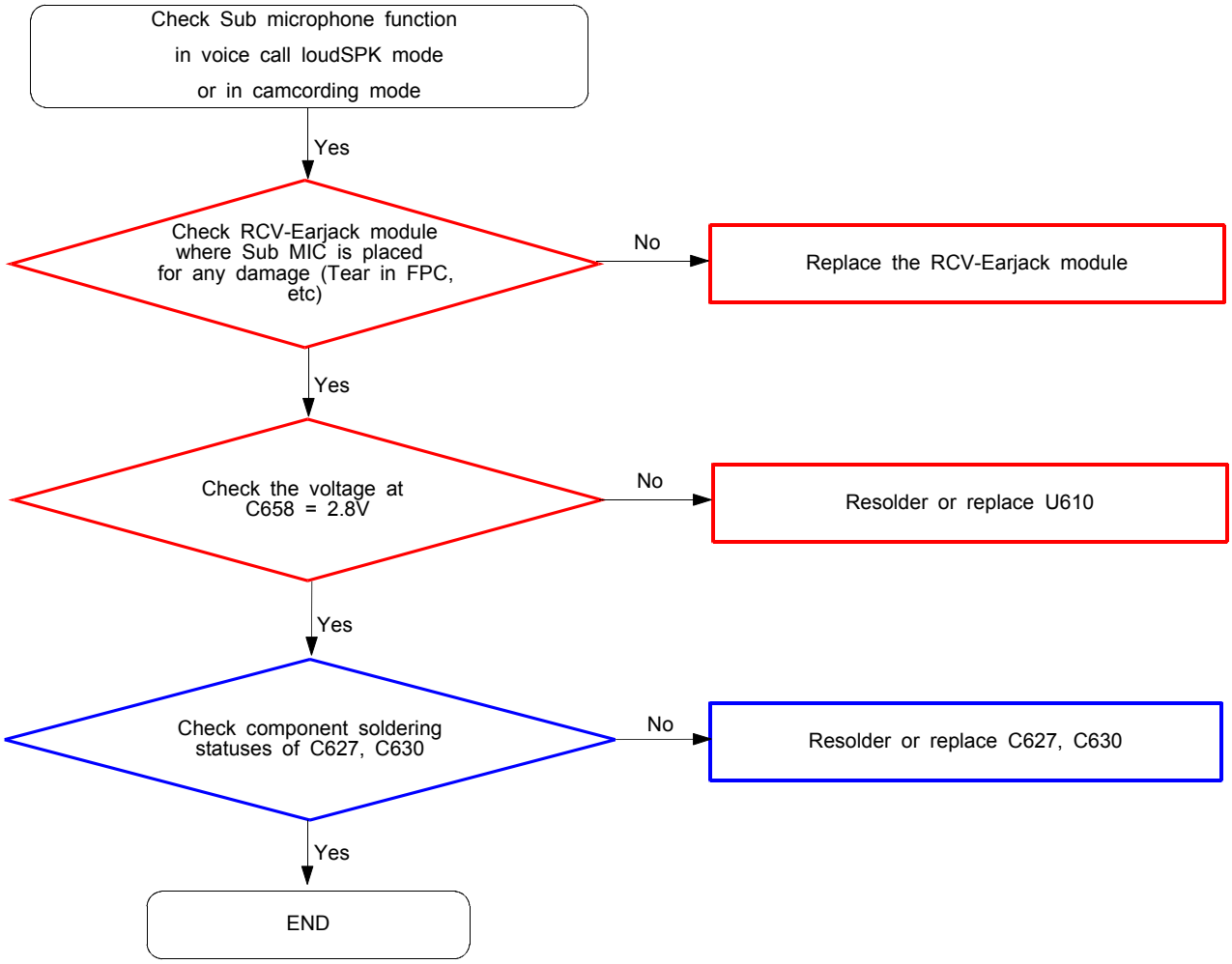
8-3-5-1. Microphone Part (Sub MIC)



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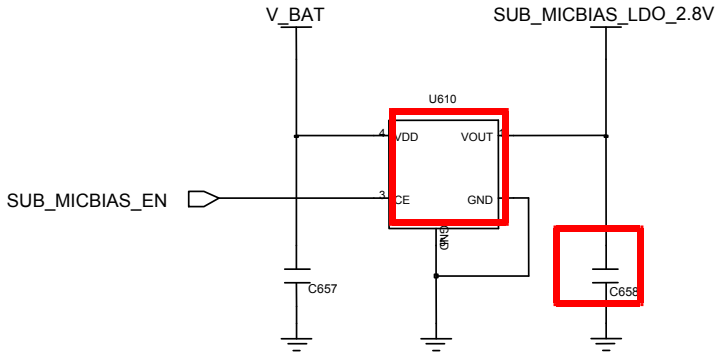

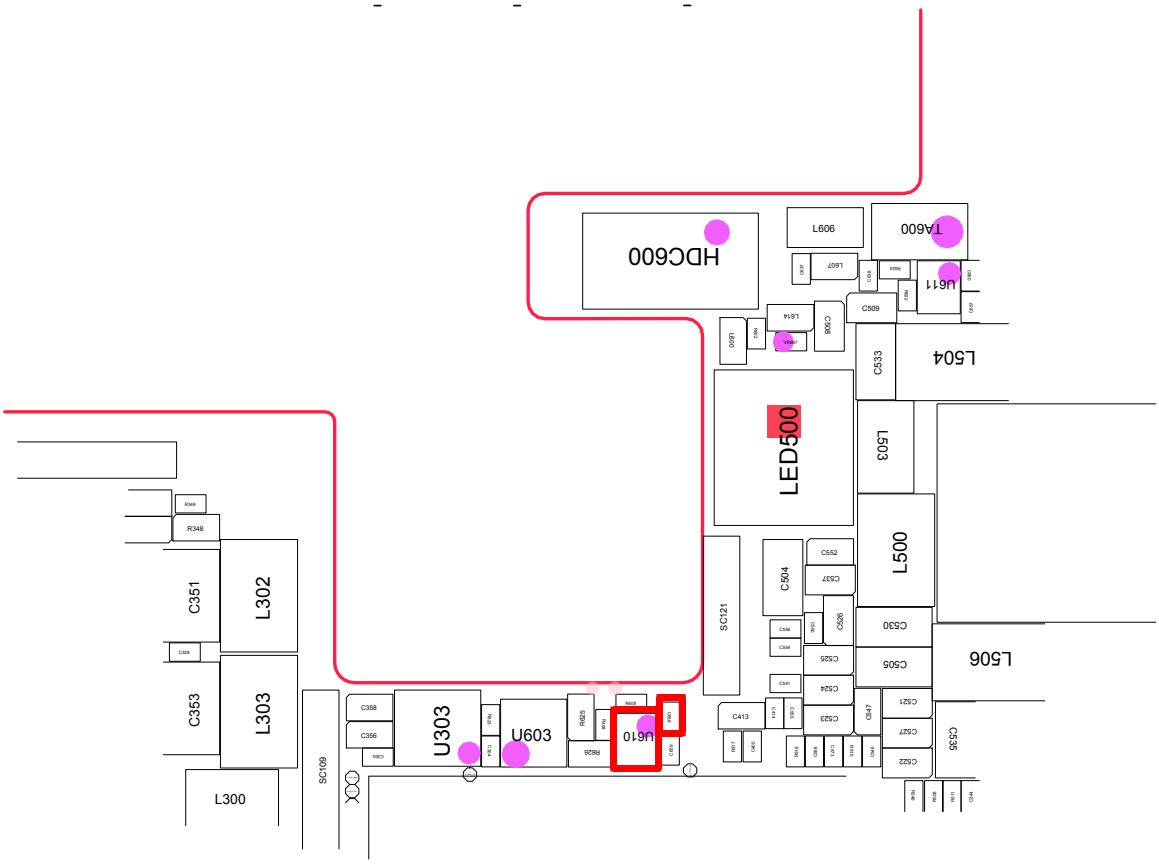

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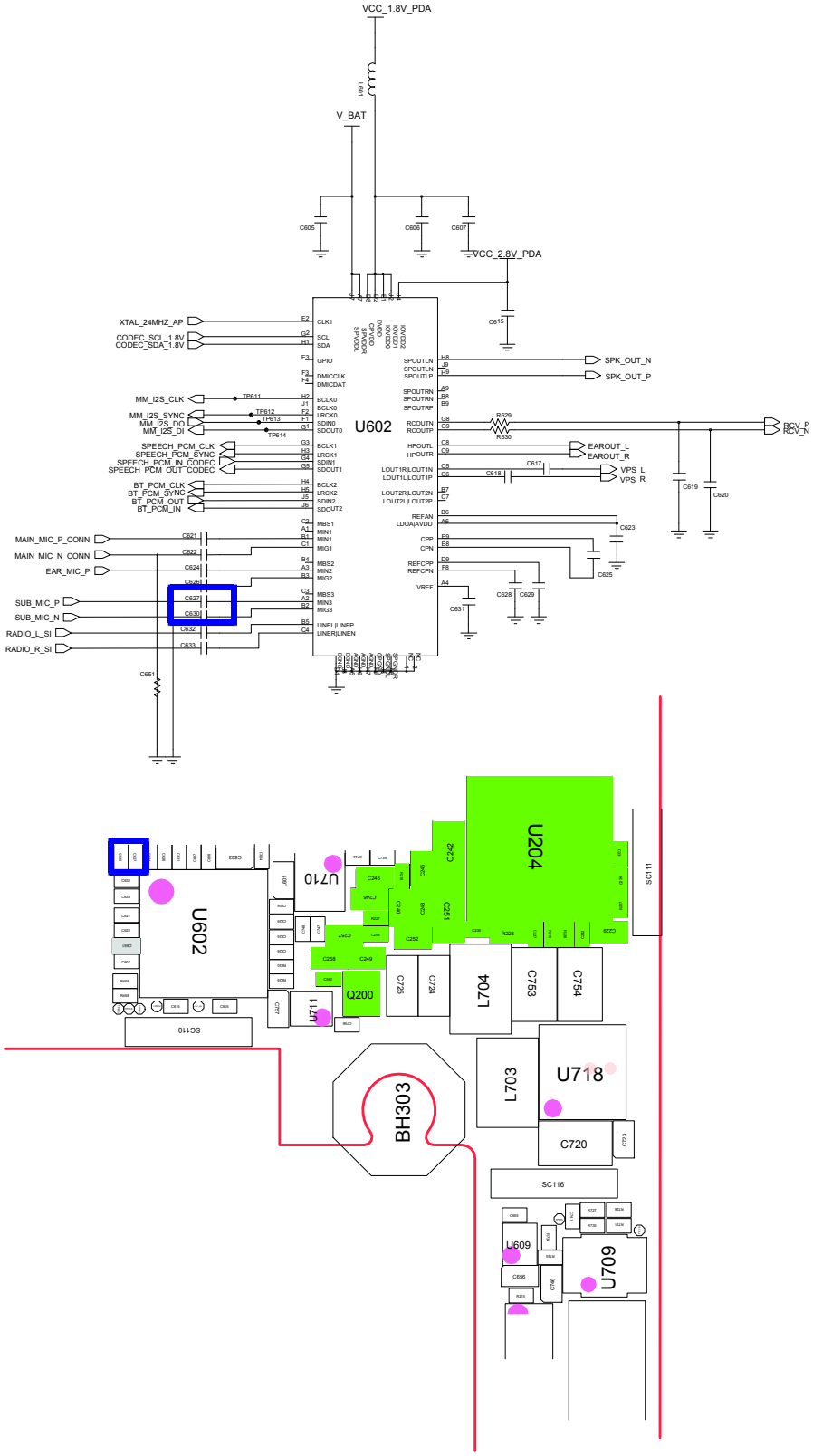

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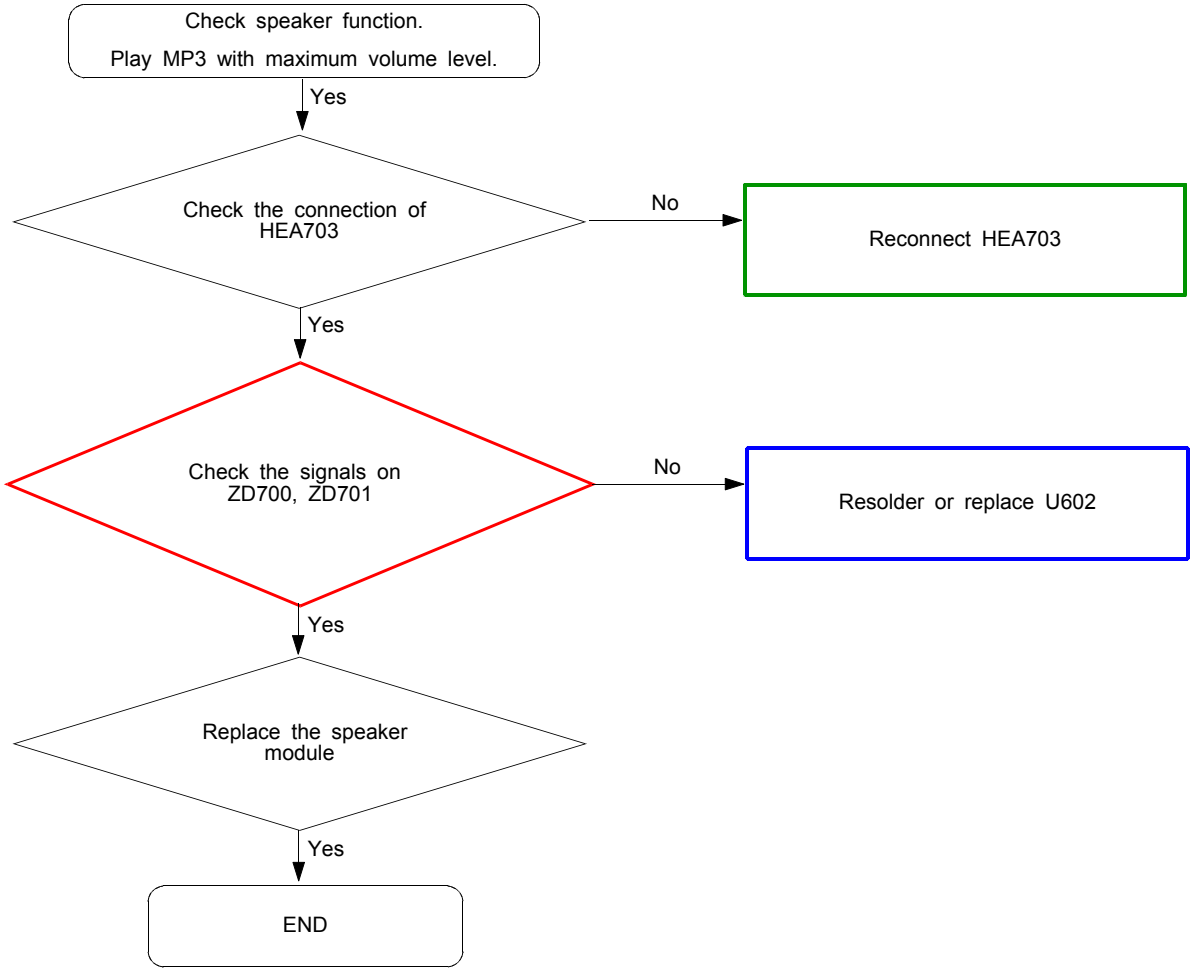
8-3-6. Speaker Part



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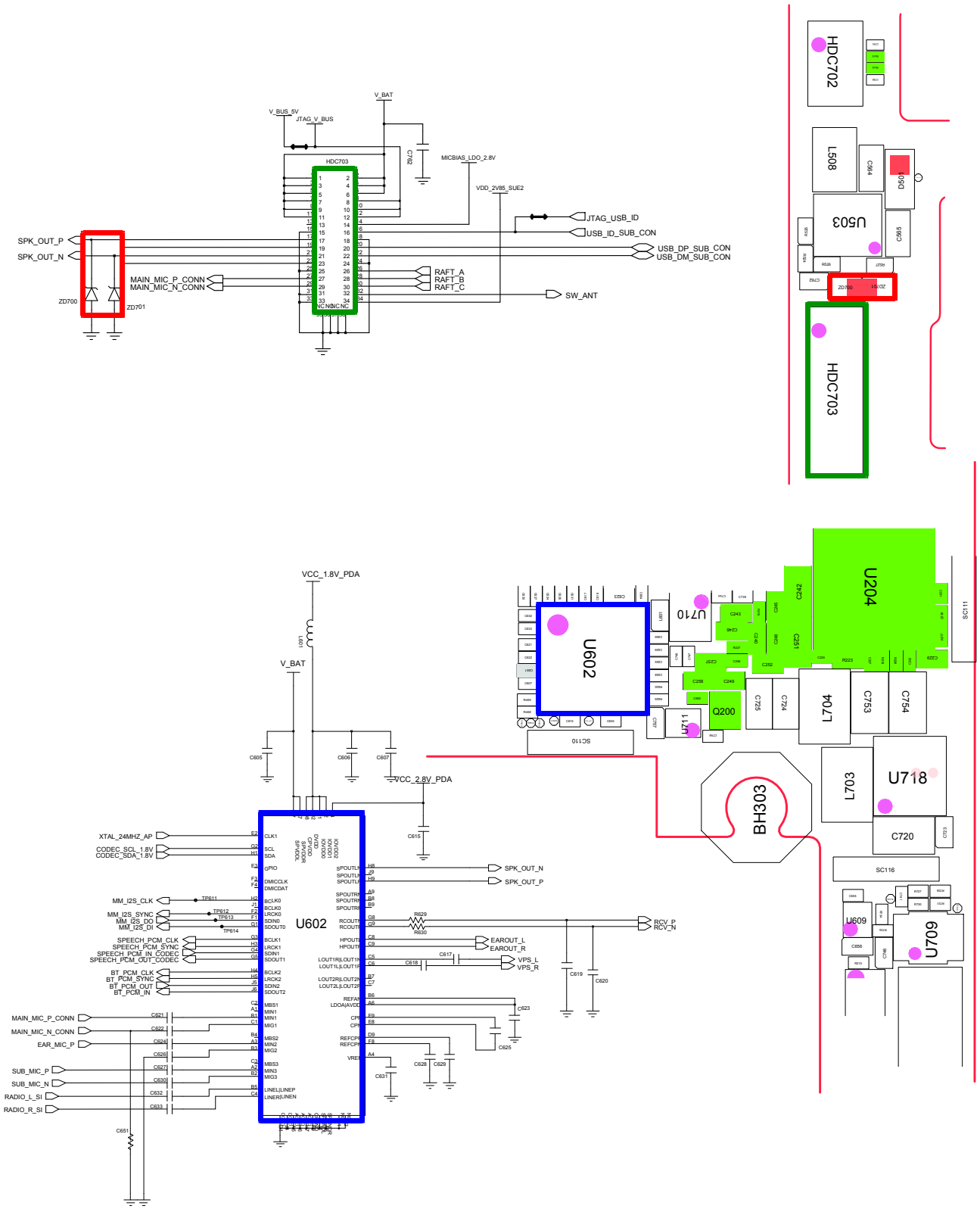

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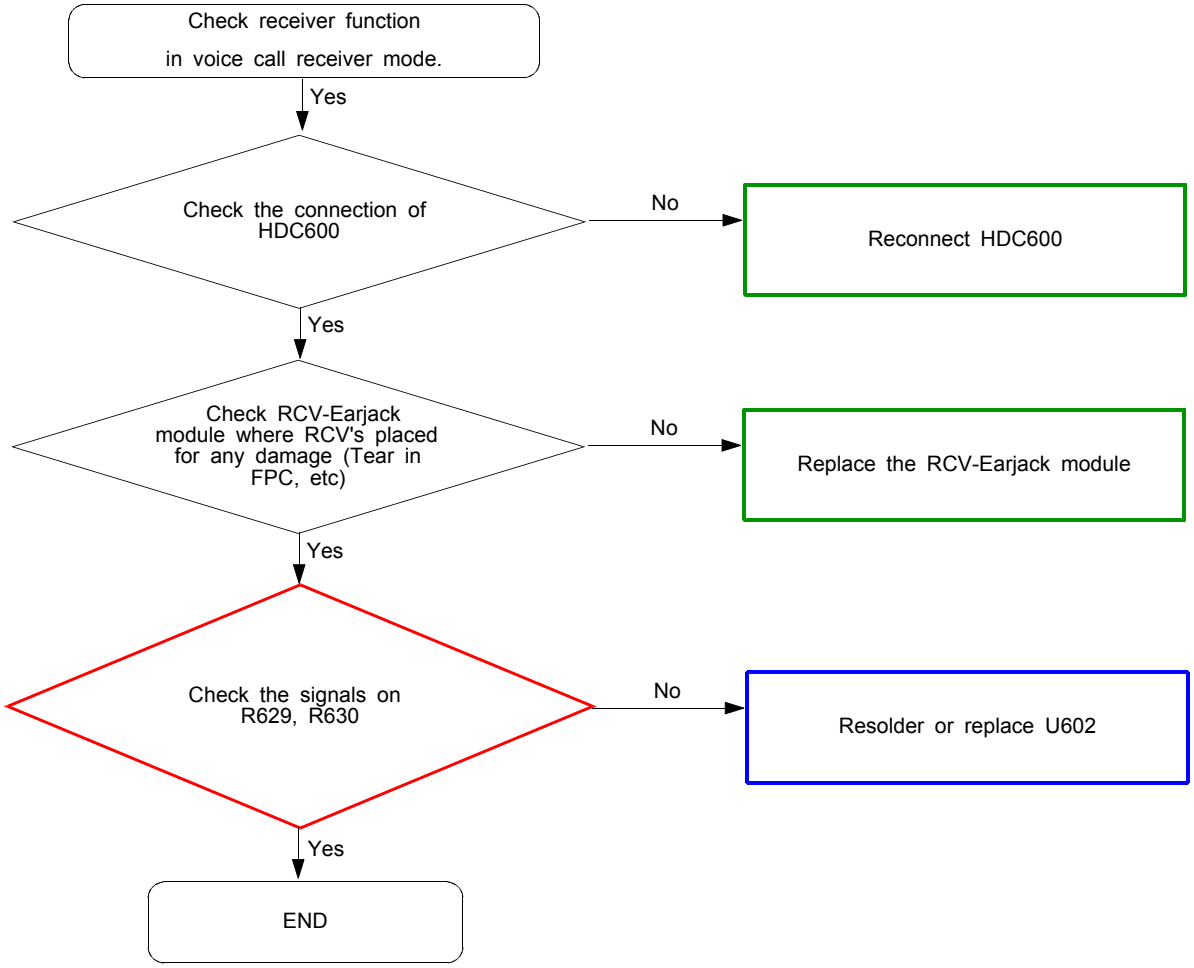
8-3-6. Receiver Part



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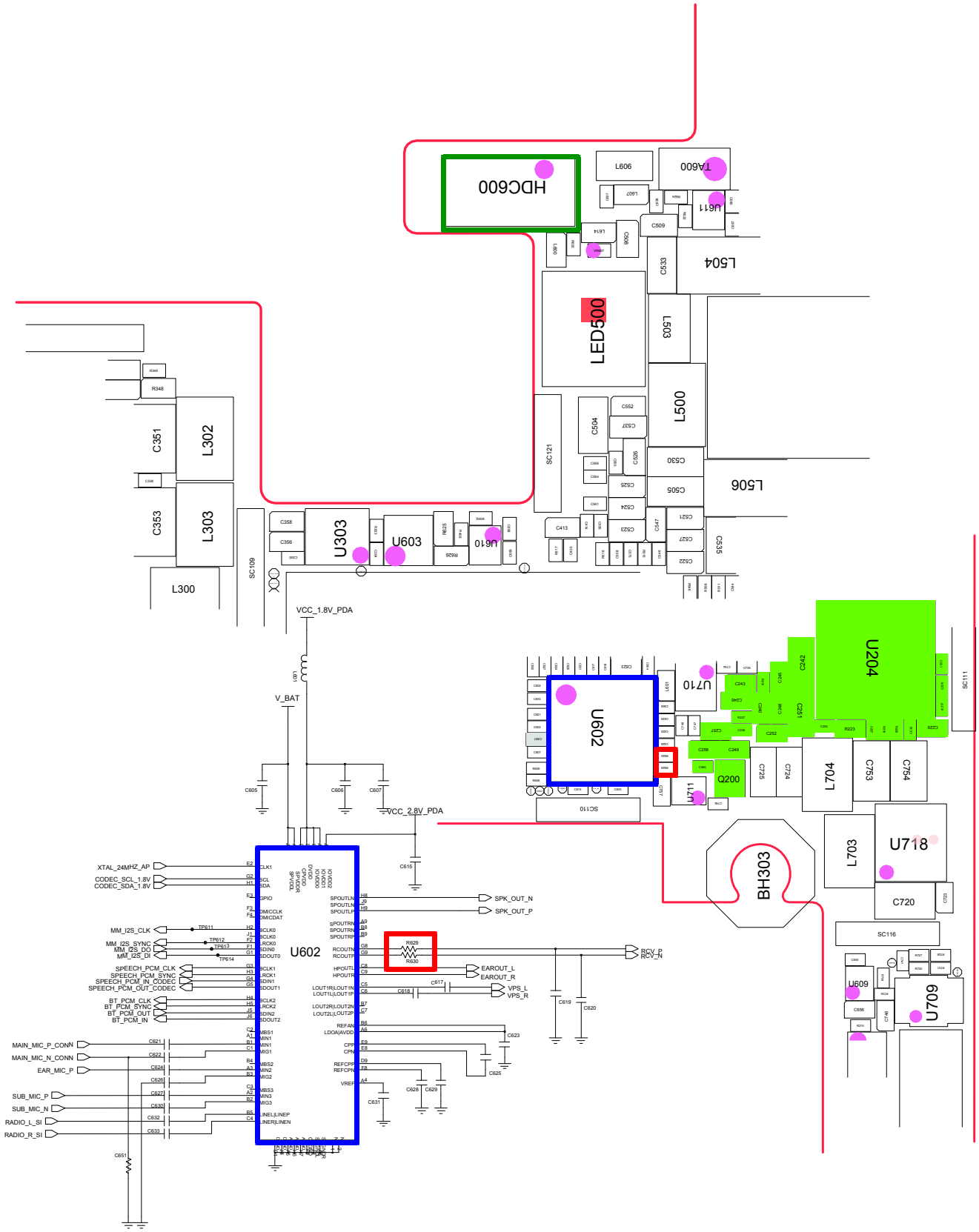

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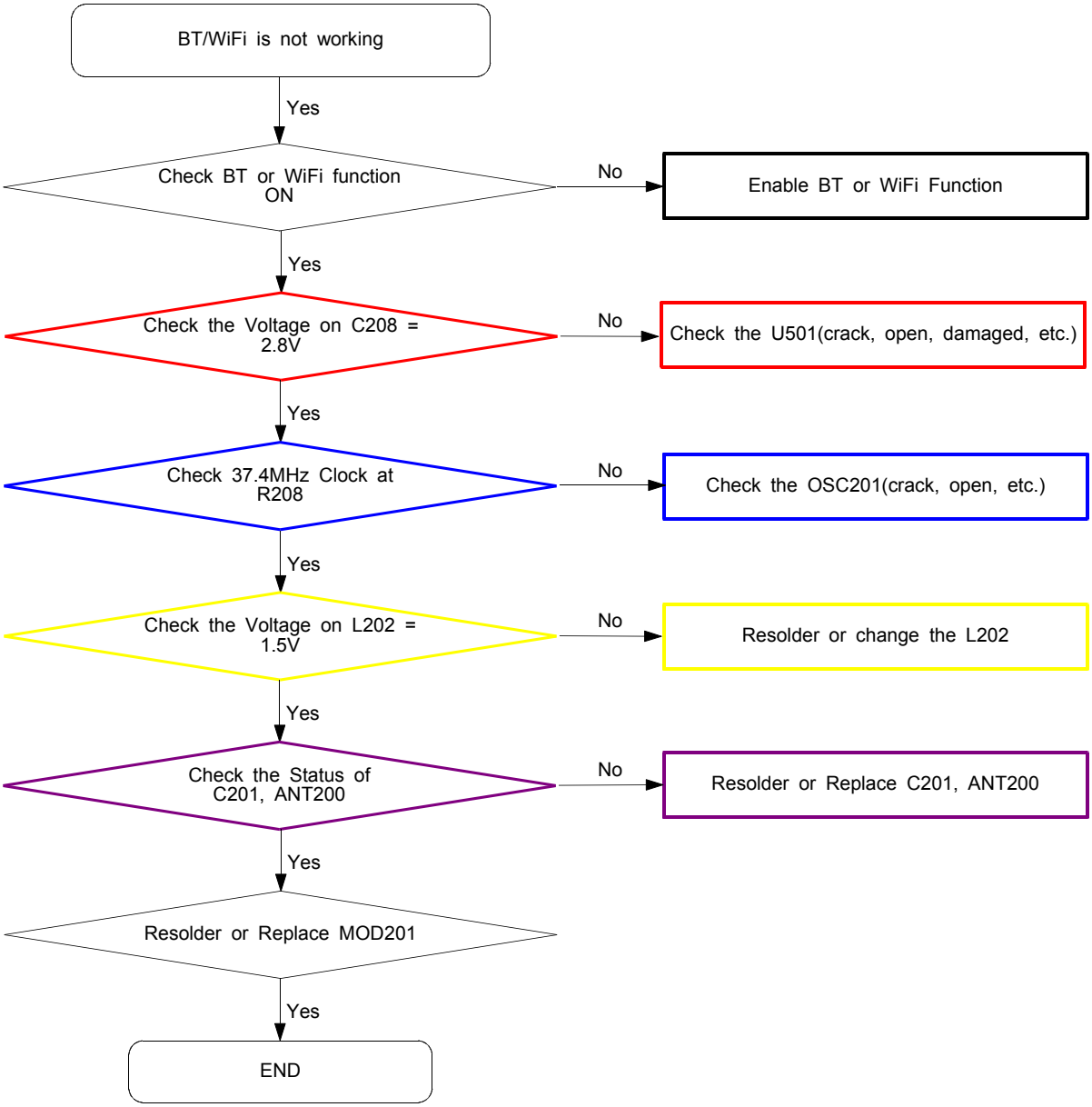
8-3-7. BT/WIFI



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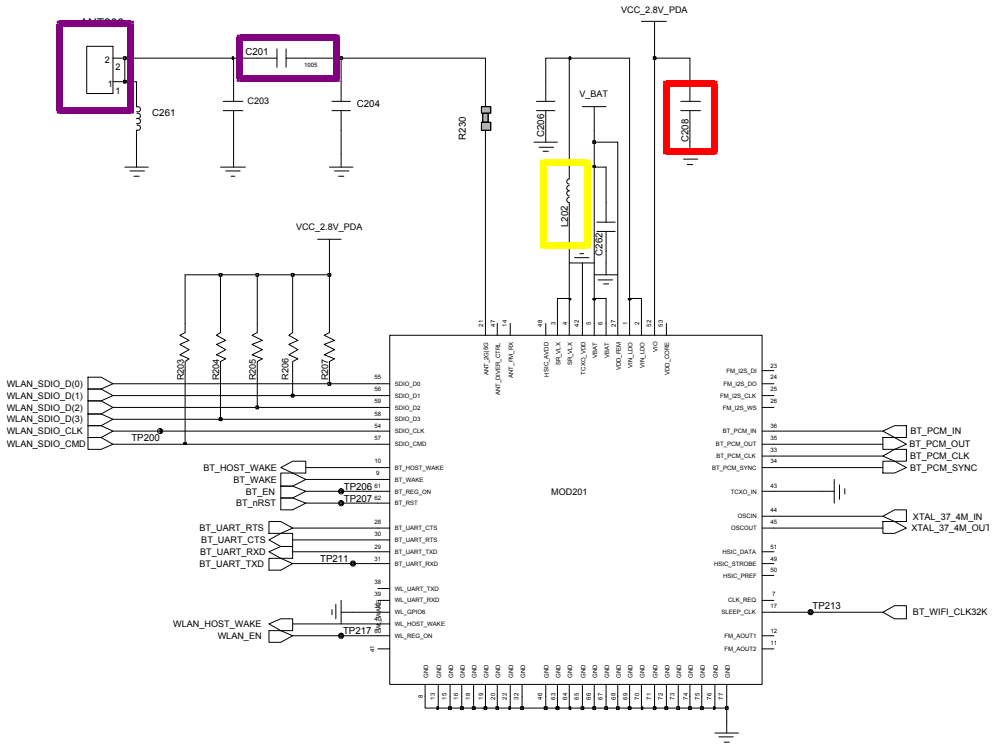

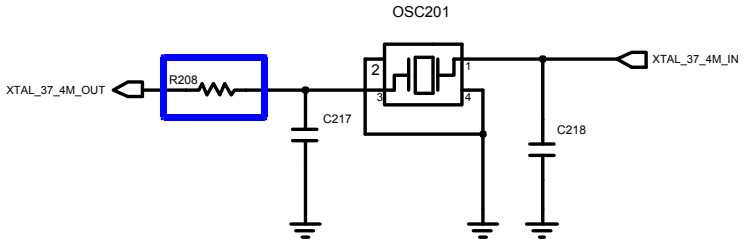

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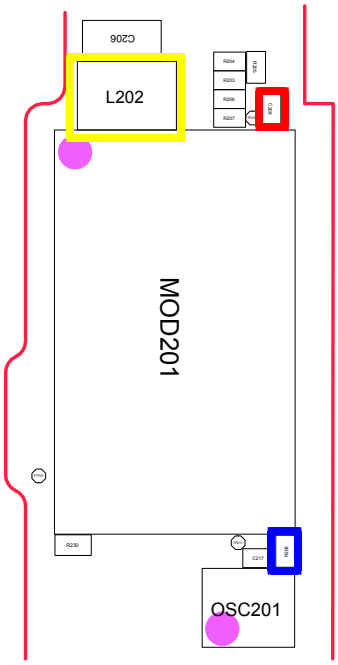

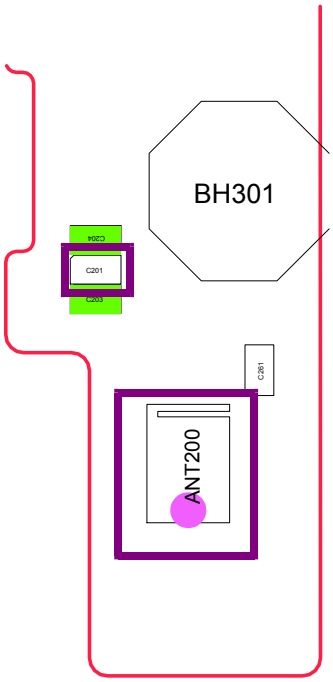

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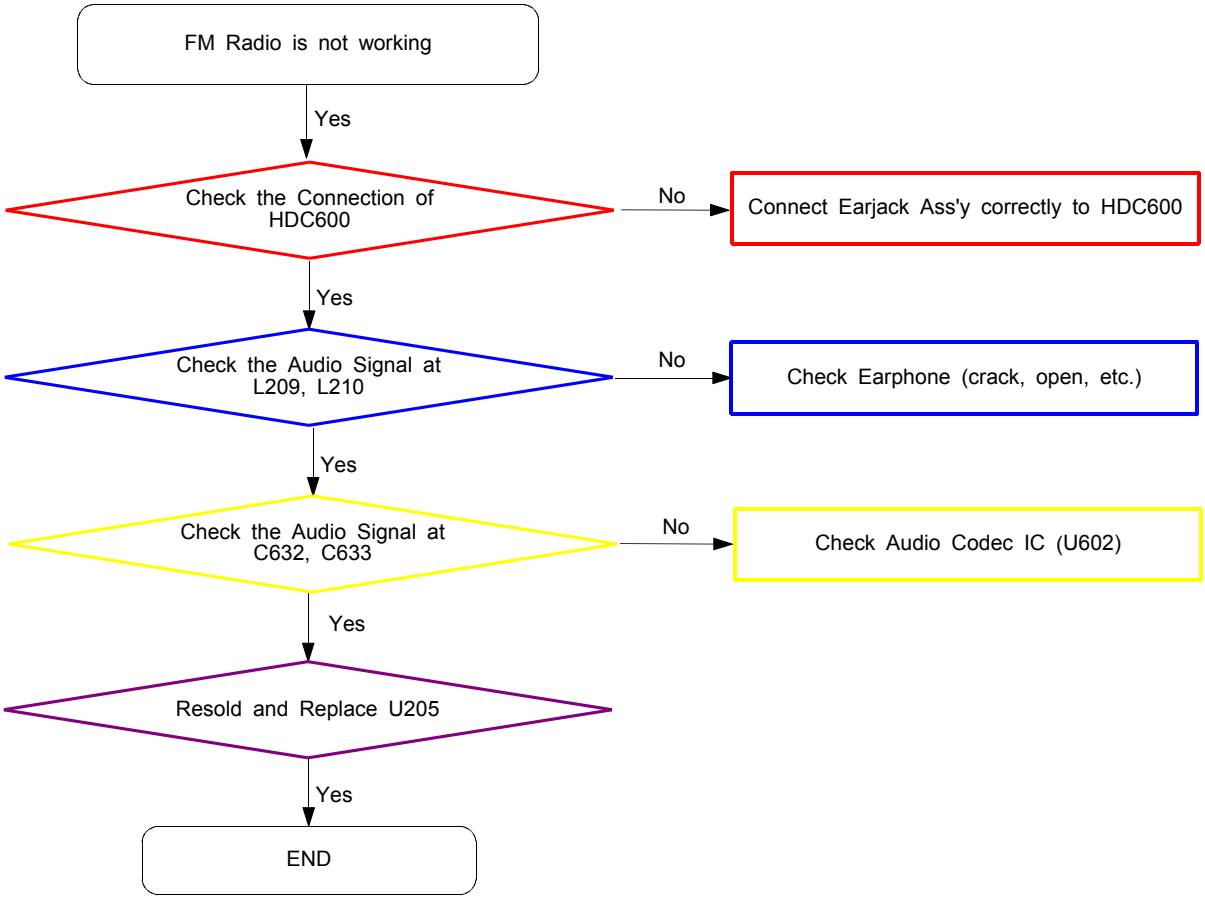
8-3-8. FM RADIO



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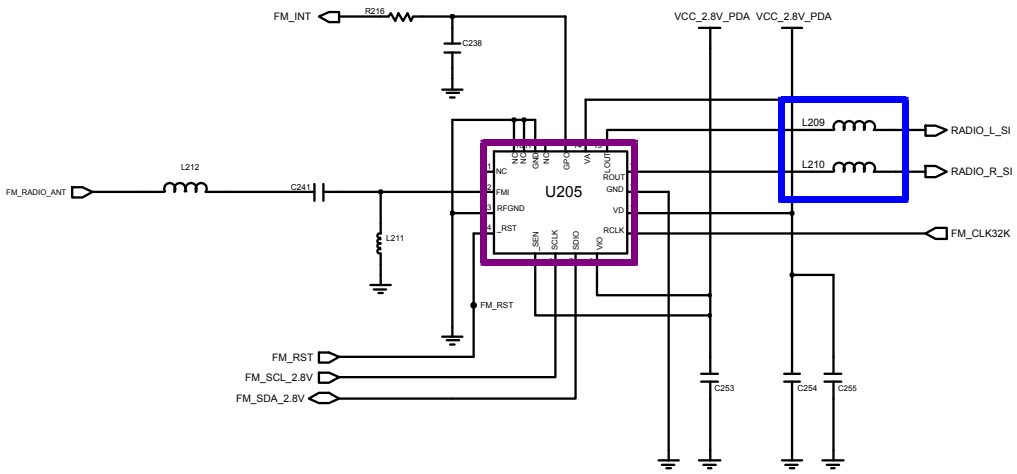

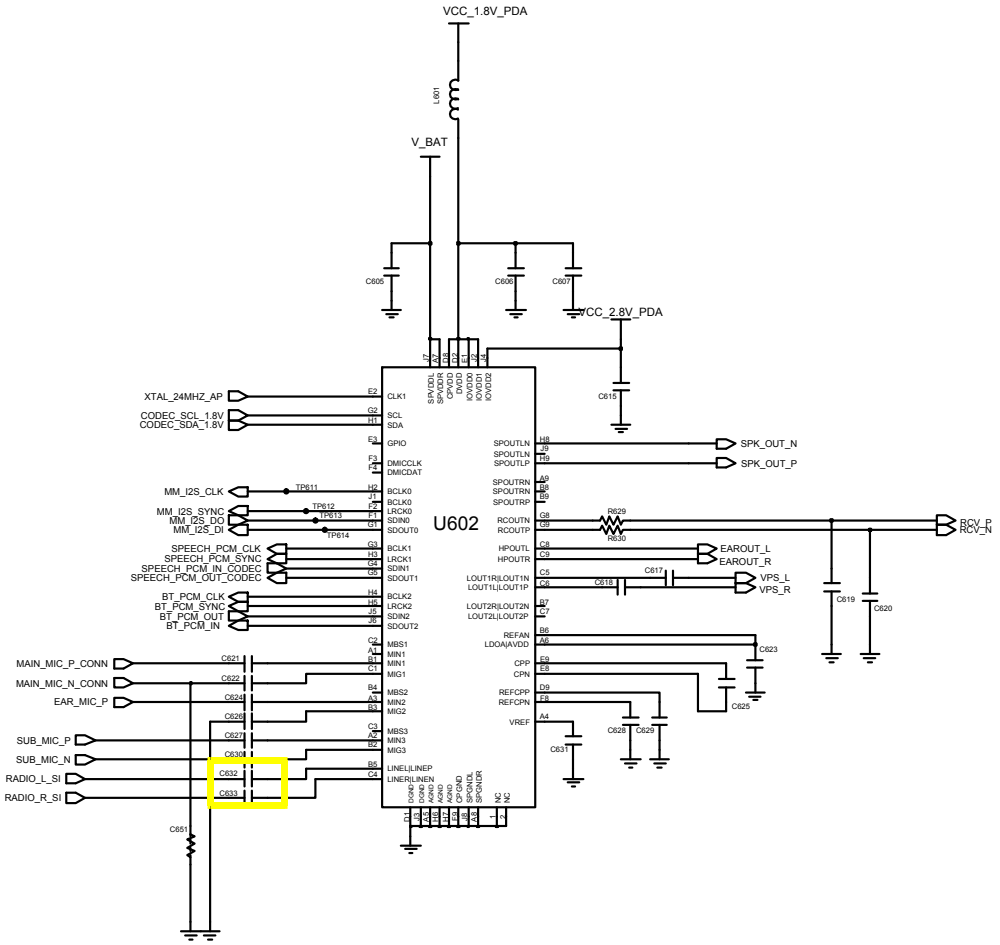

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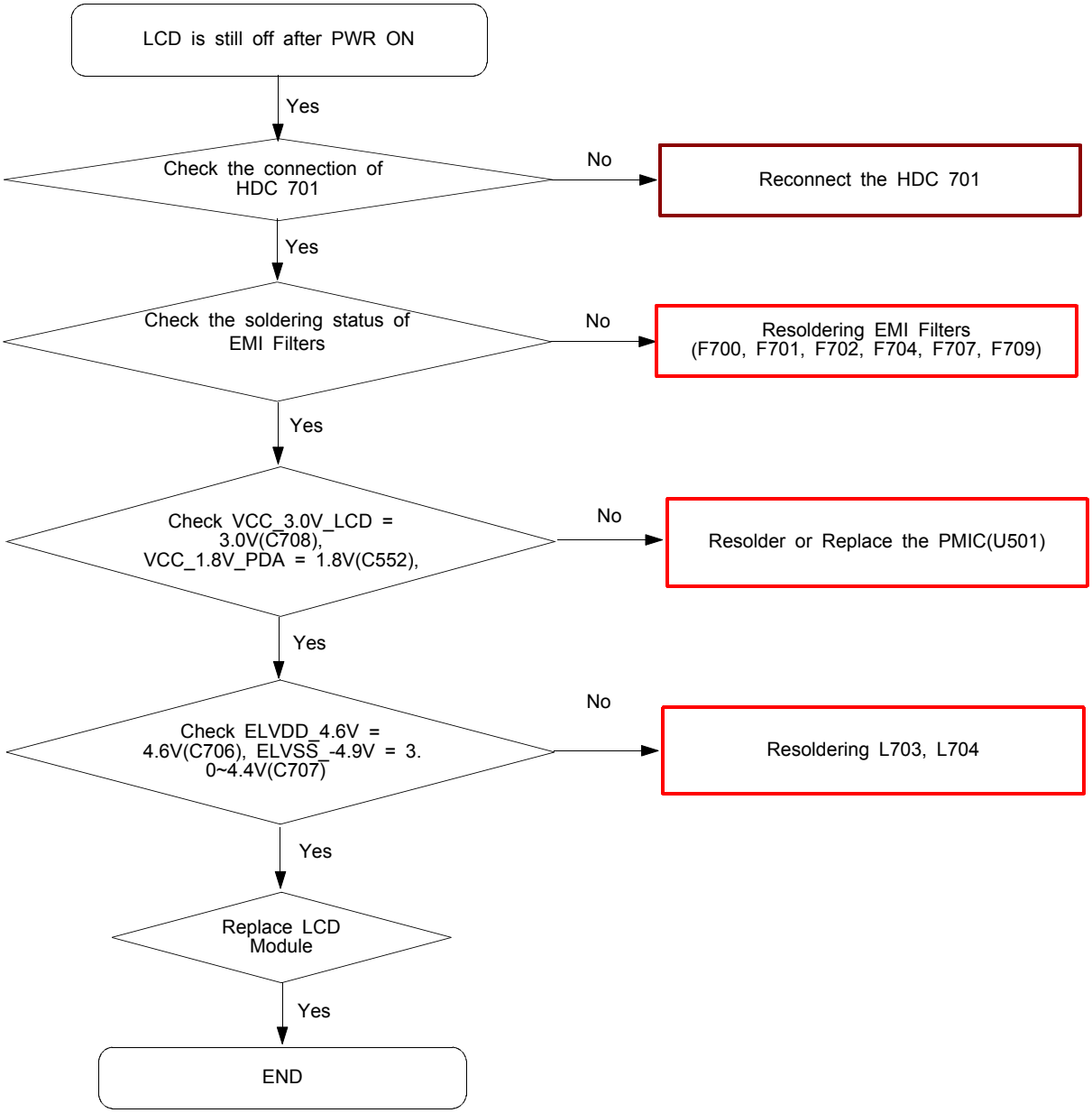
8-3-8. LCD



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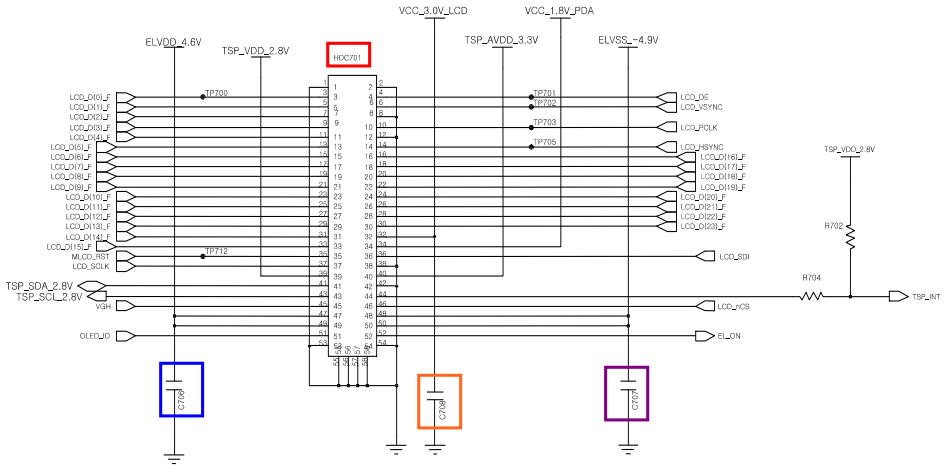

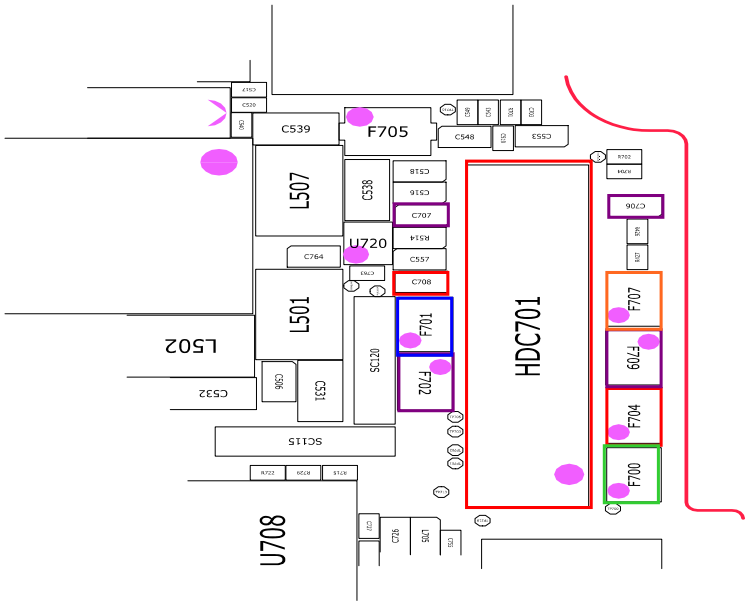

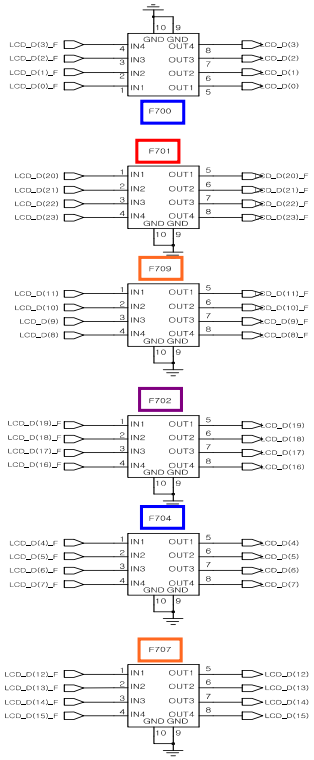

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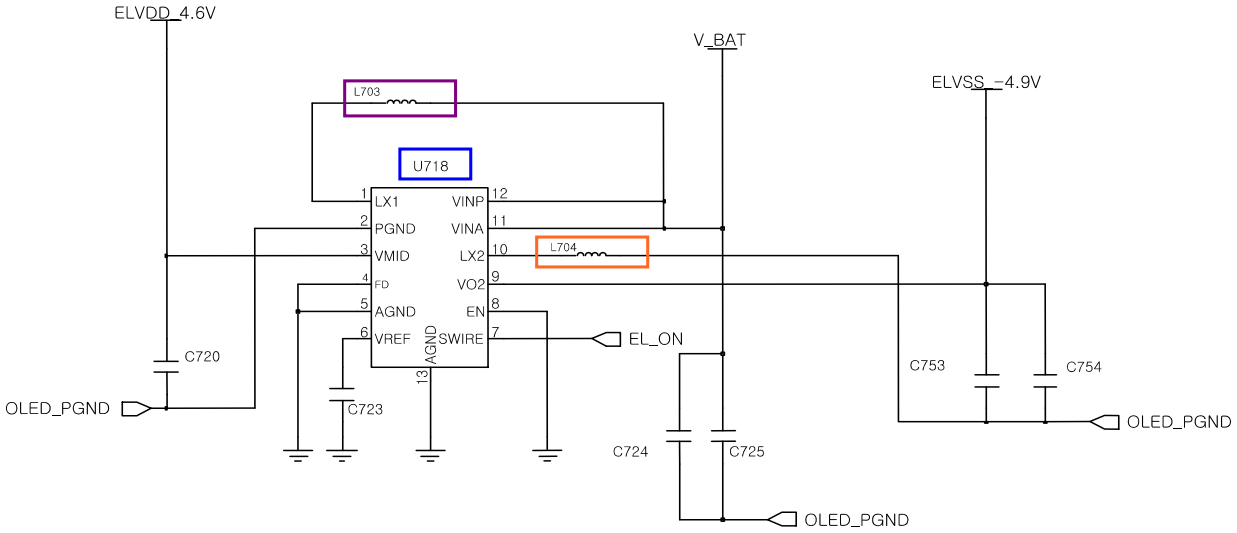

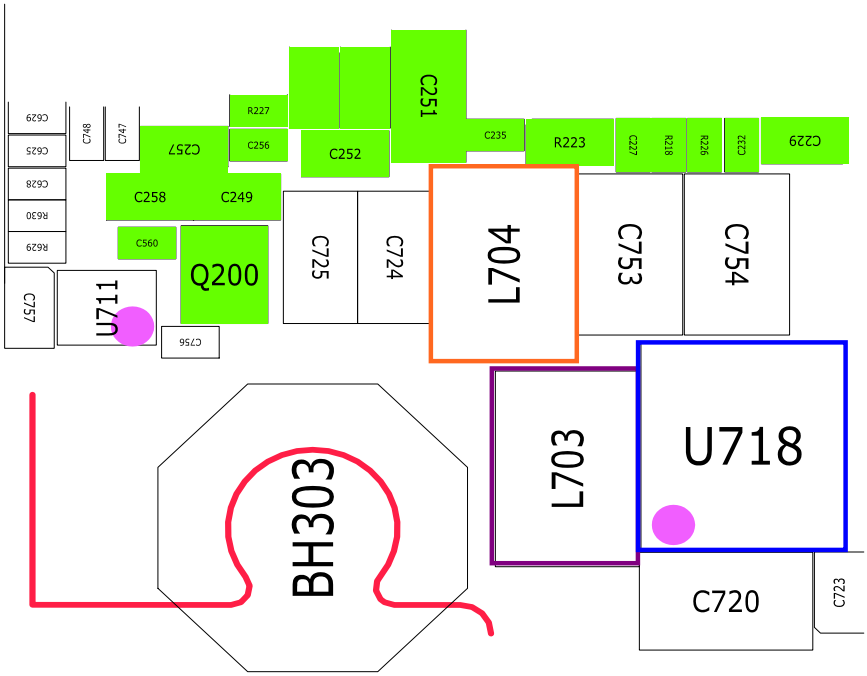

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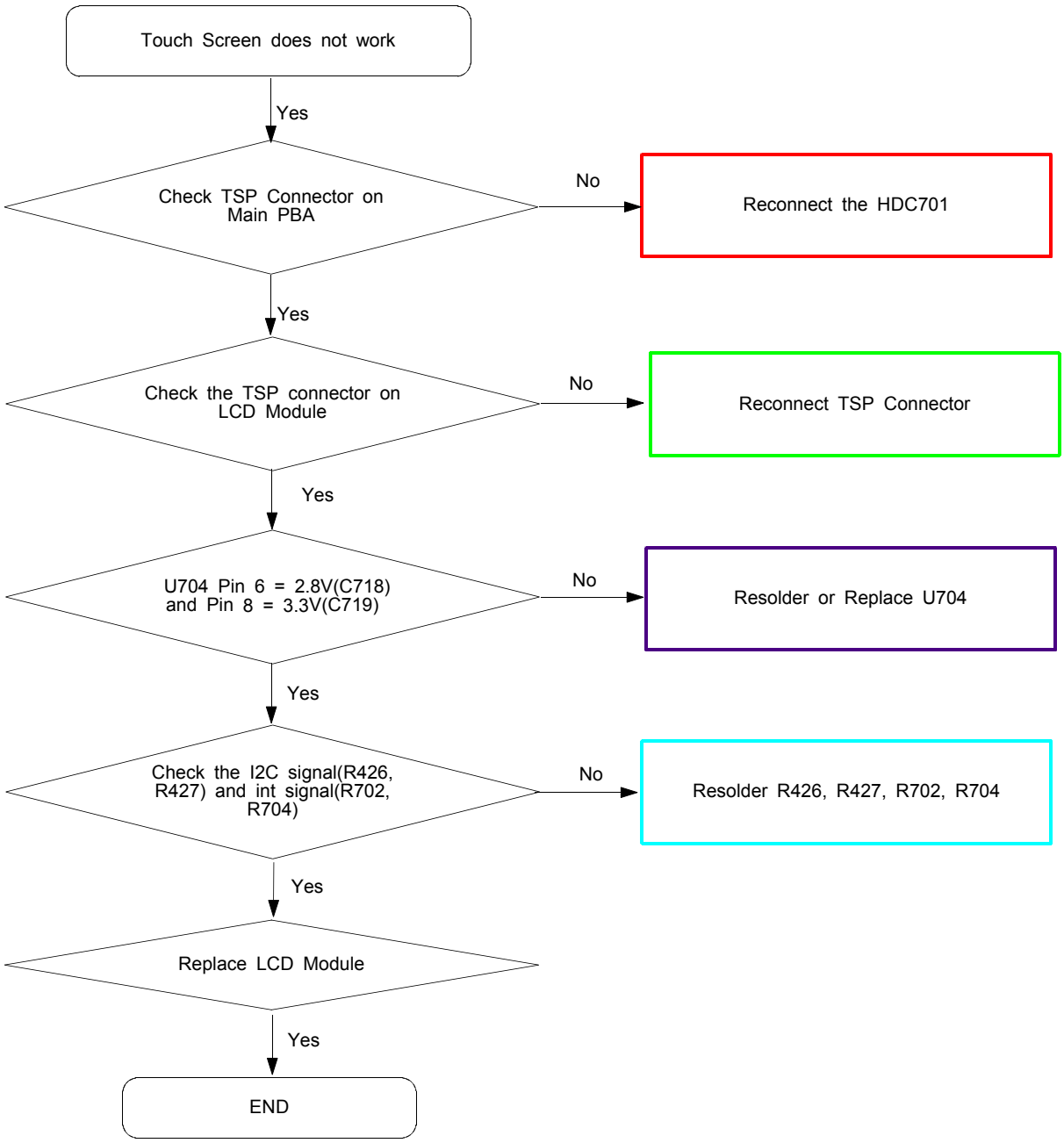
8-3-9. TSP



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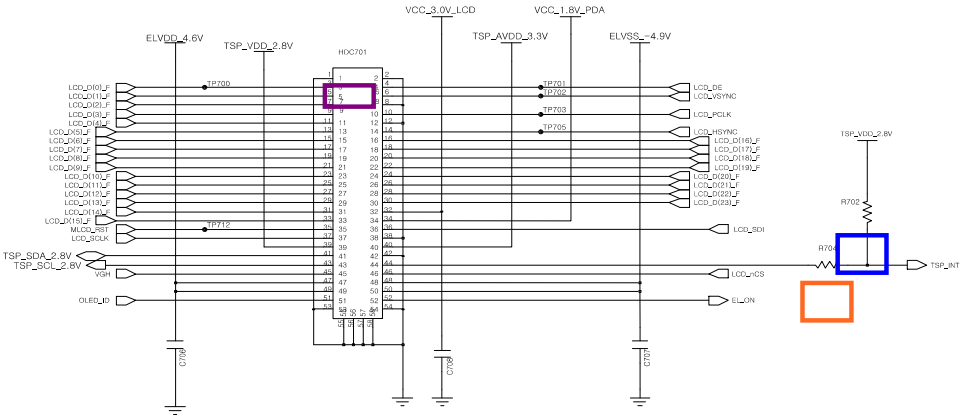

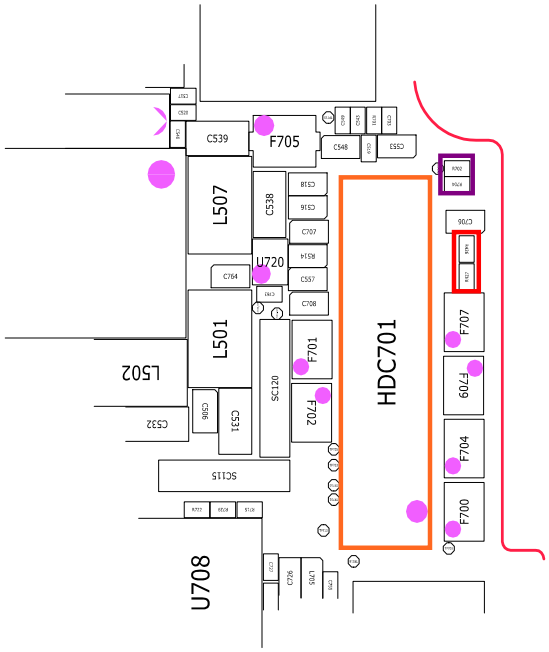

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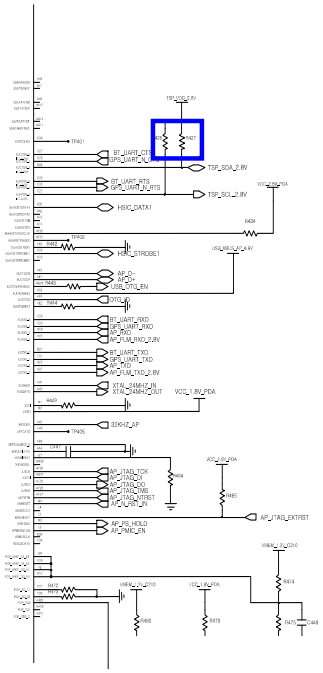

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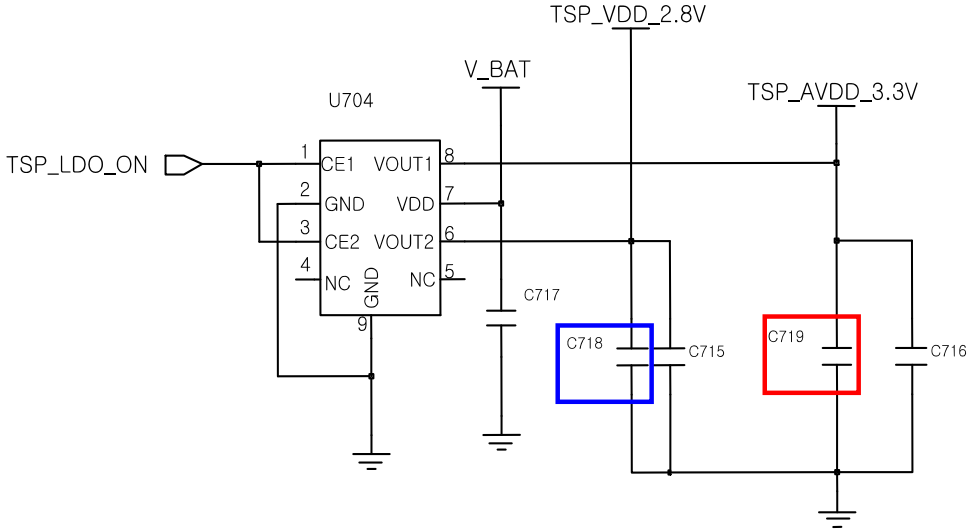

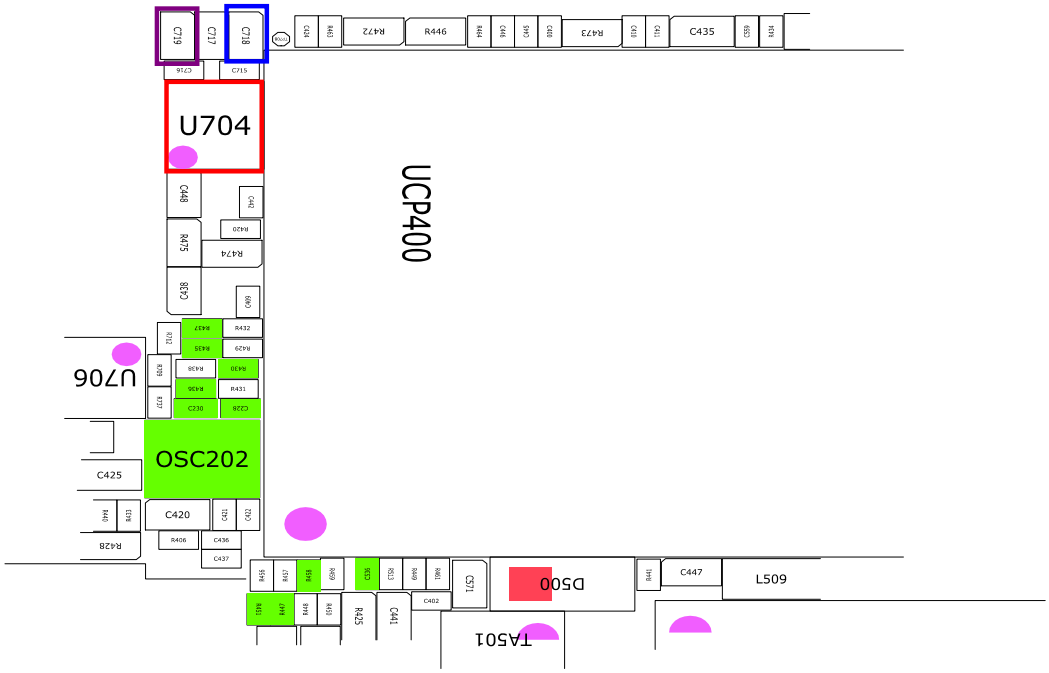

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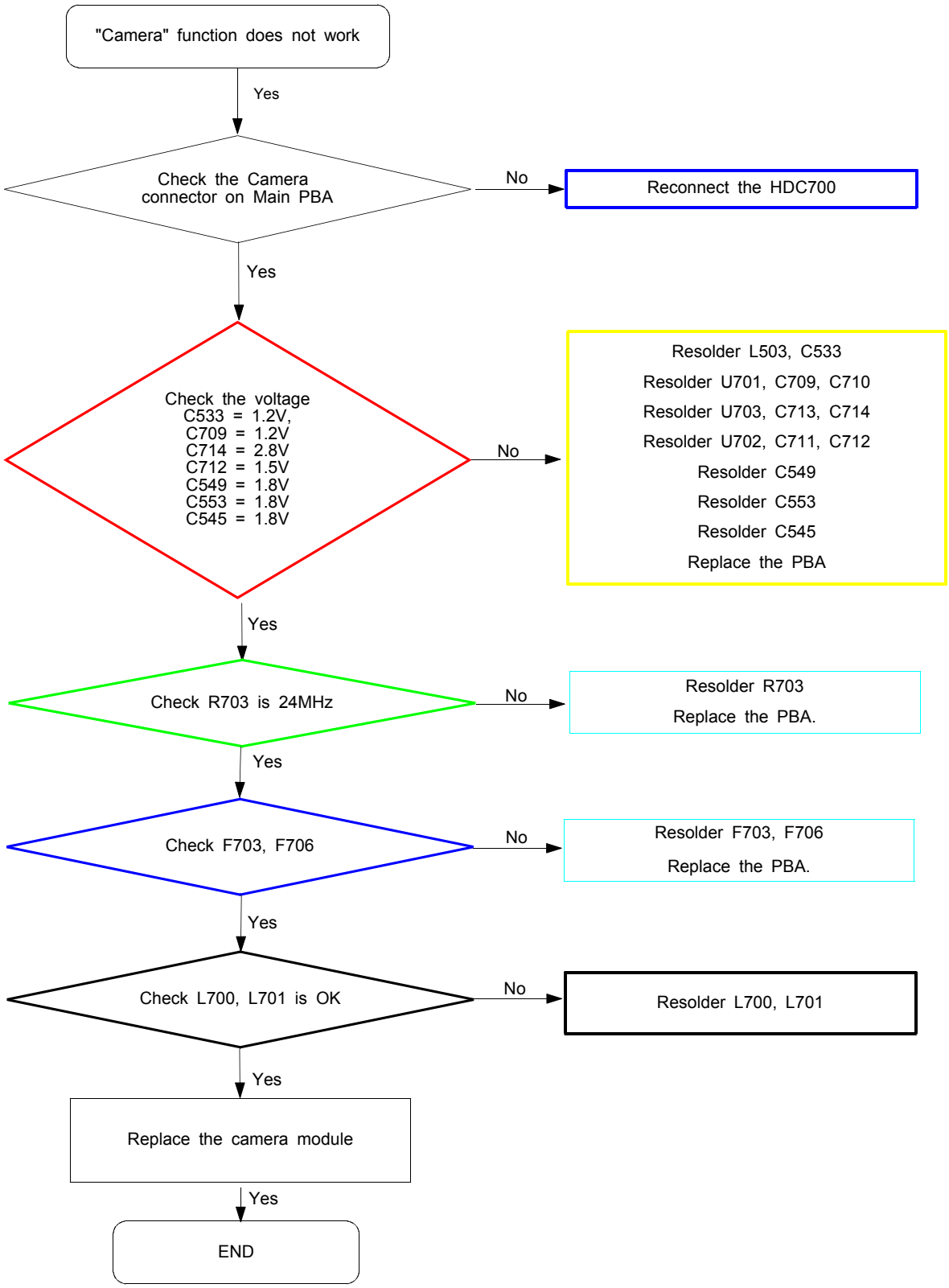
8-3-10. 8M CAM



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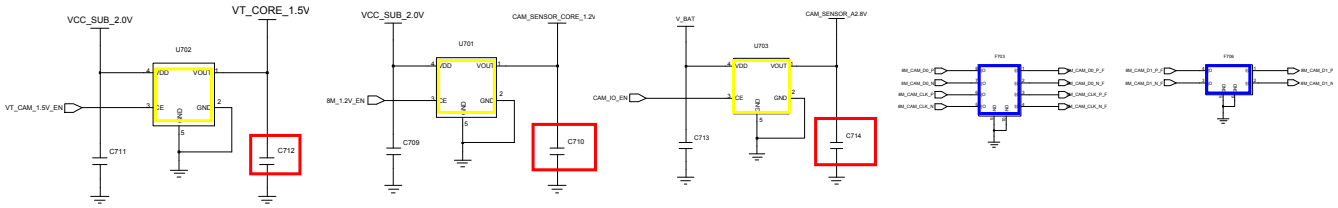

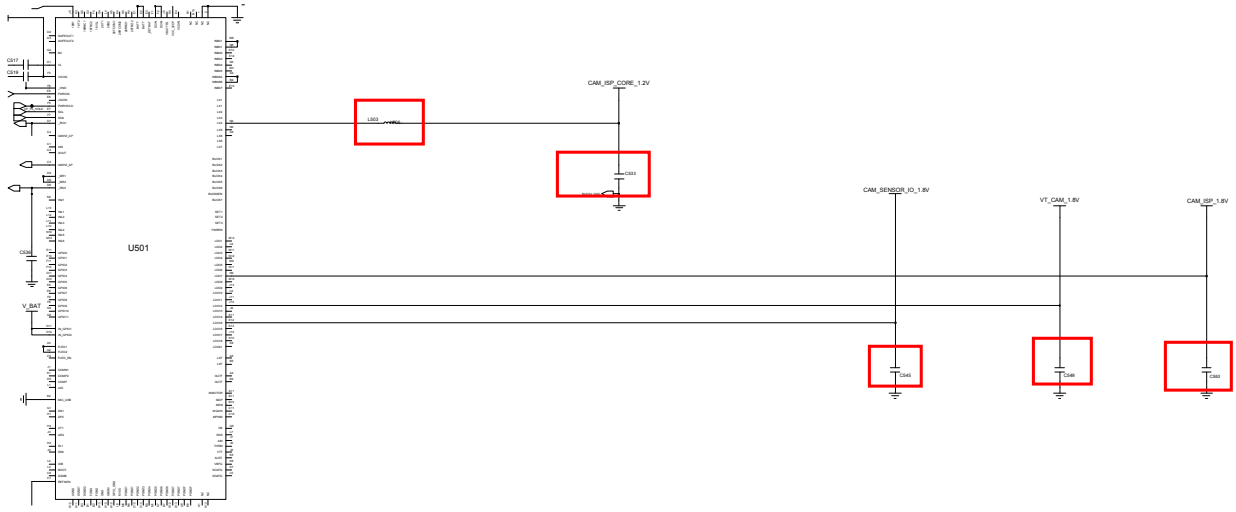

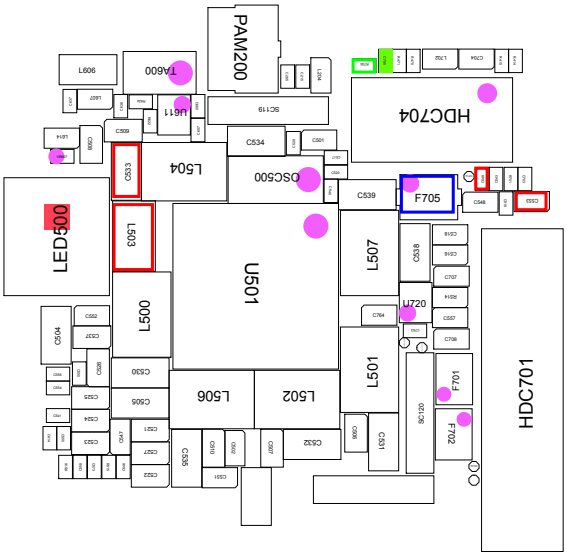

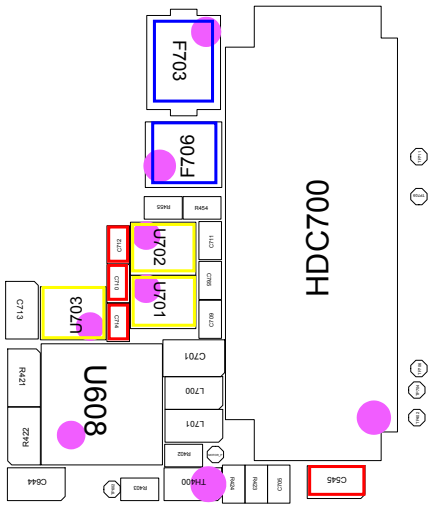

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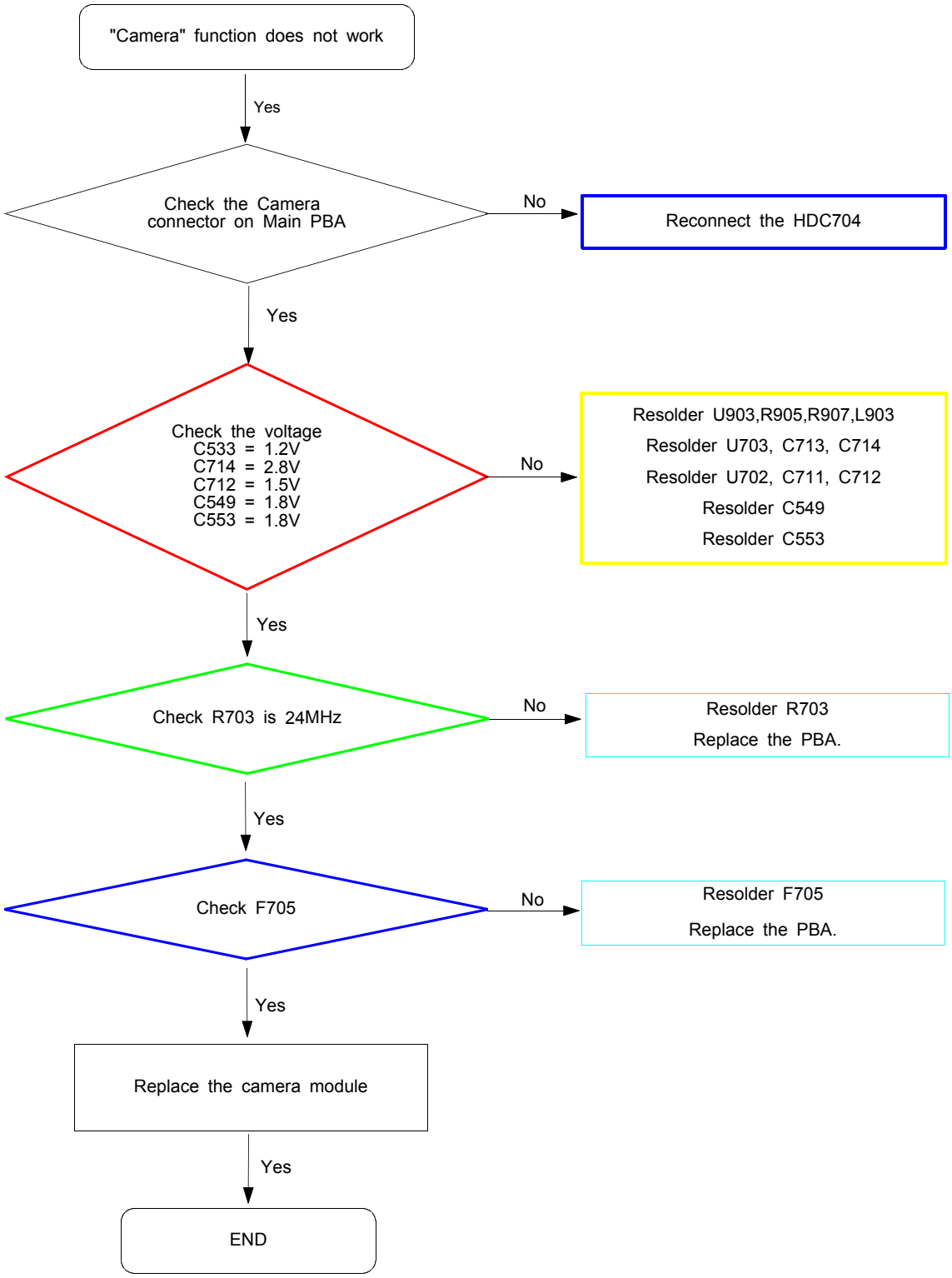
8-3-11. 2M CAM



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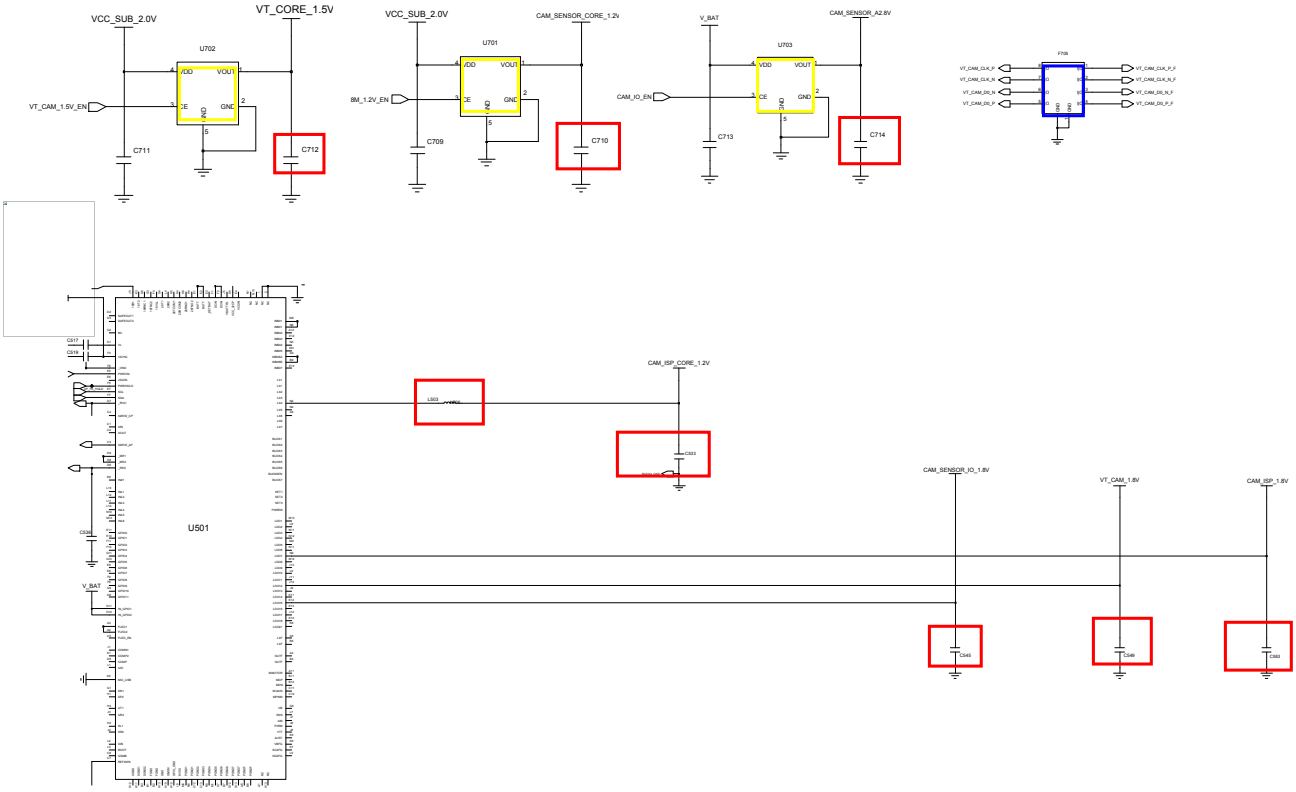

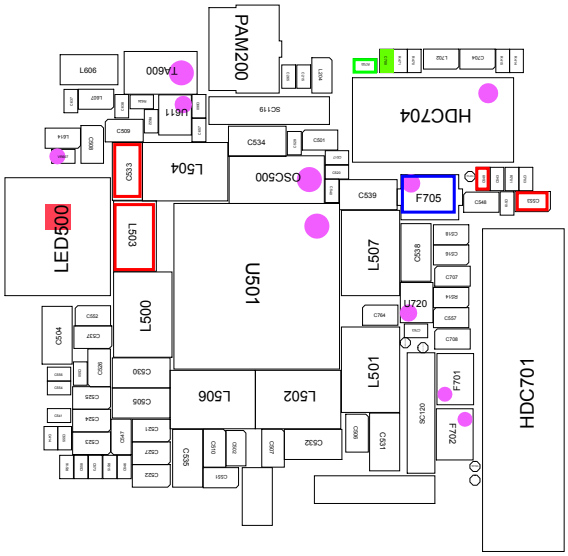

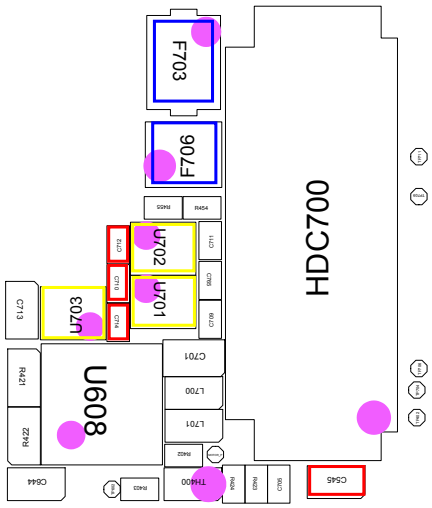

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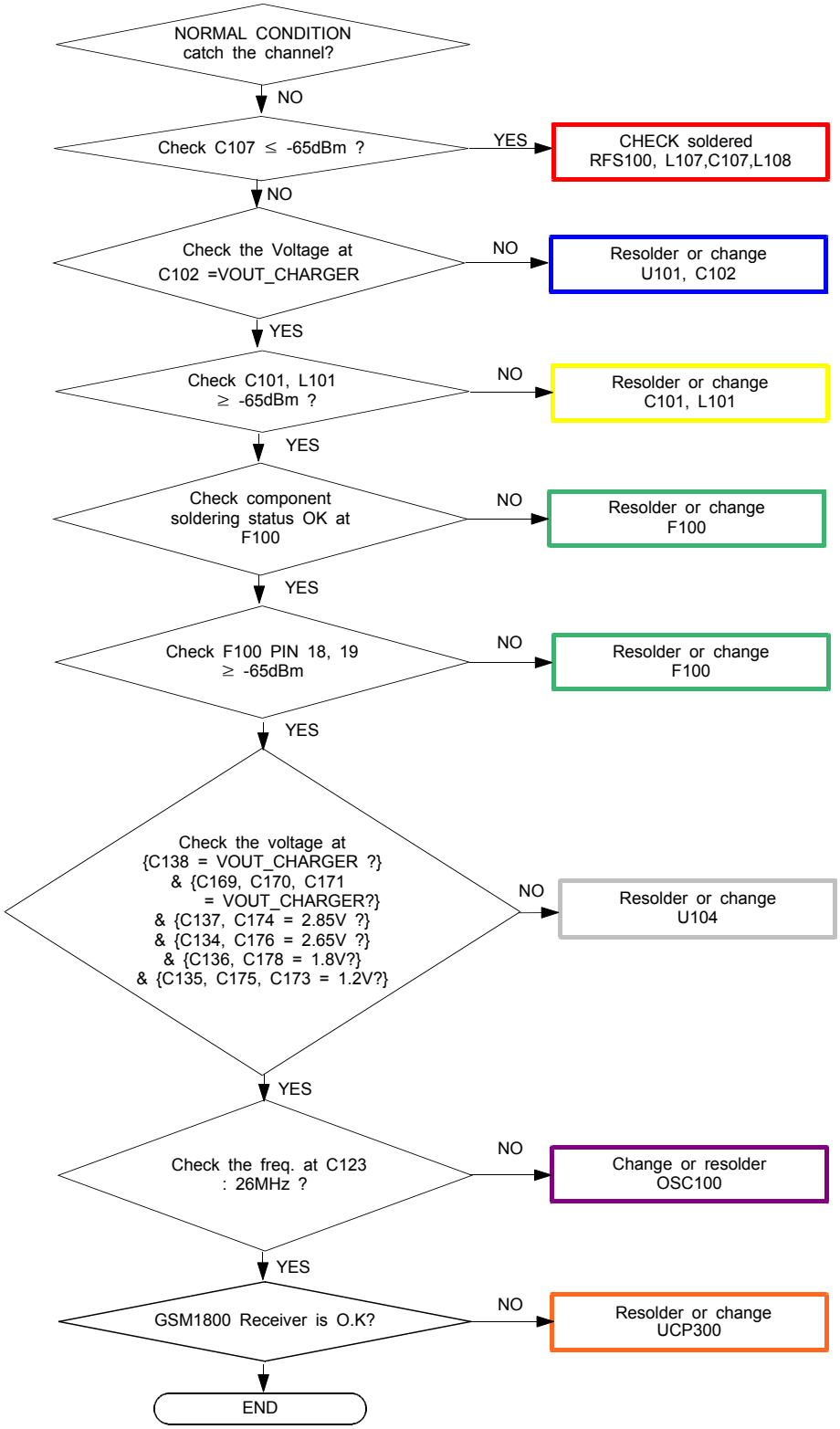
8-3-12. GSM1800 RX



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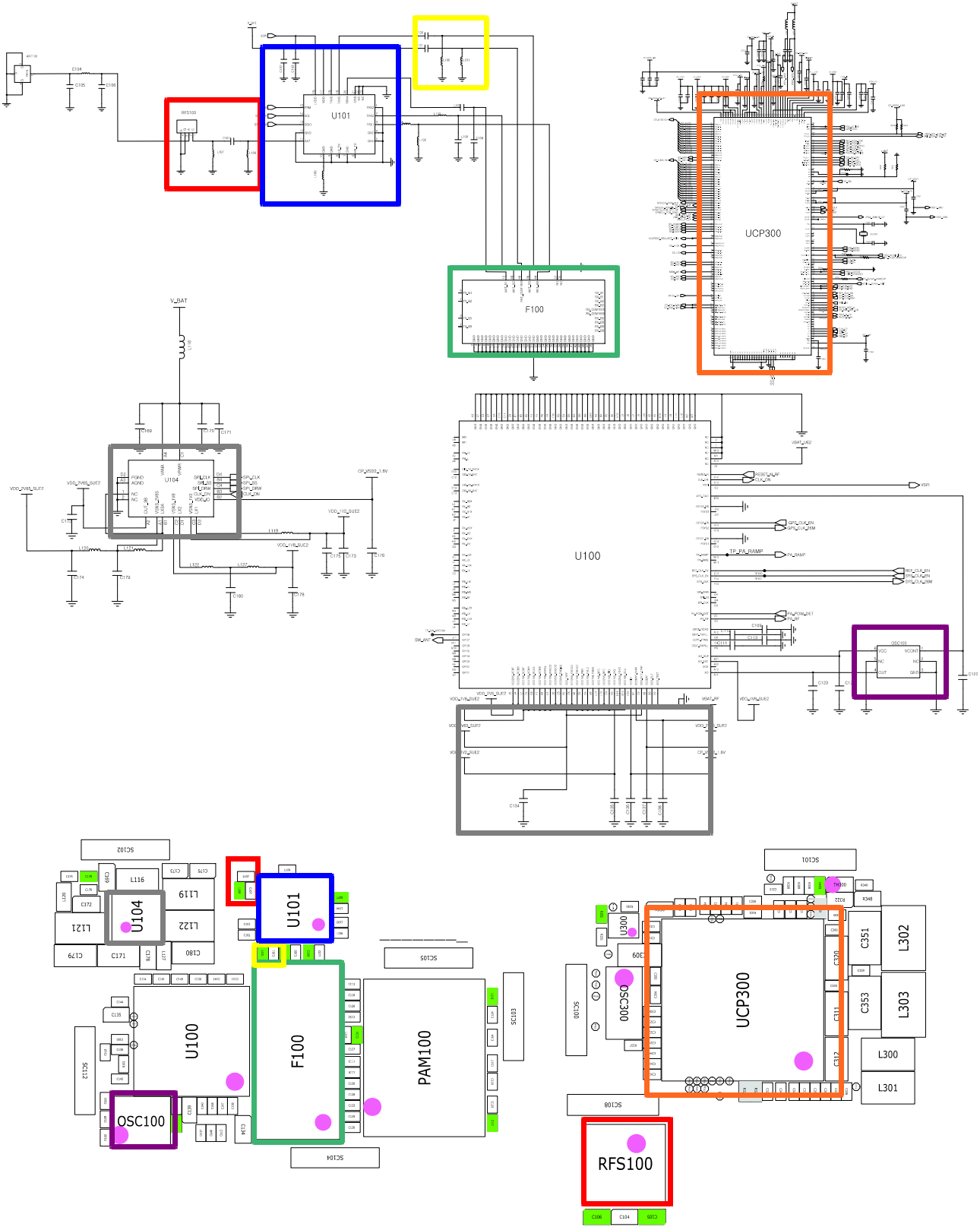

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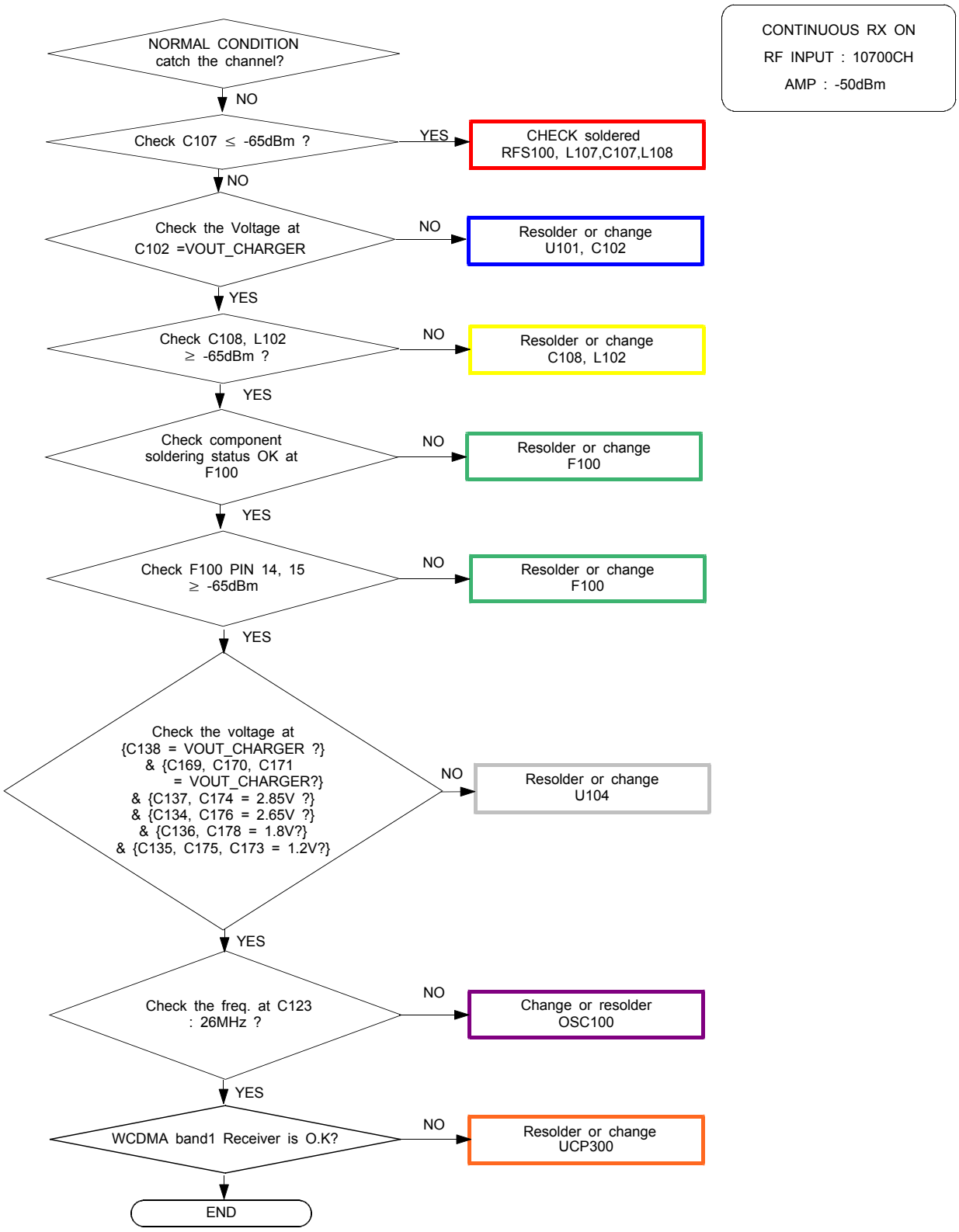
8-3-13. WCDMA Band1 RX



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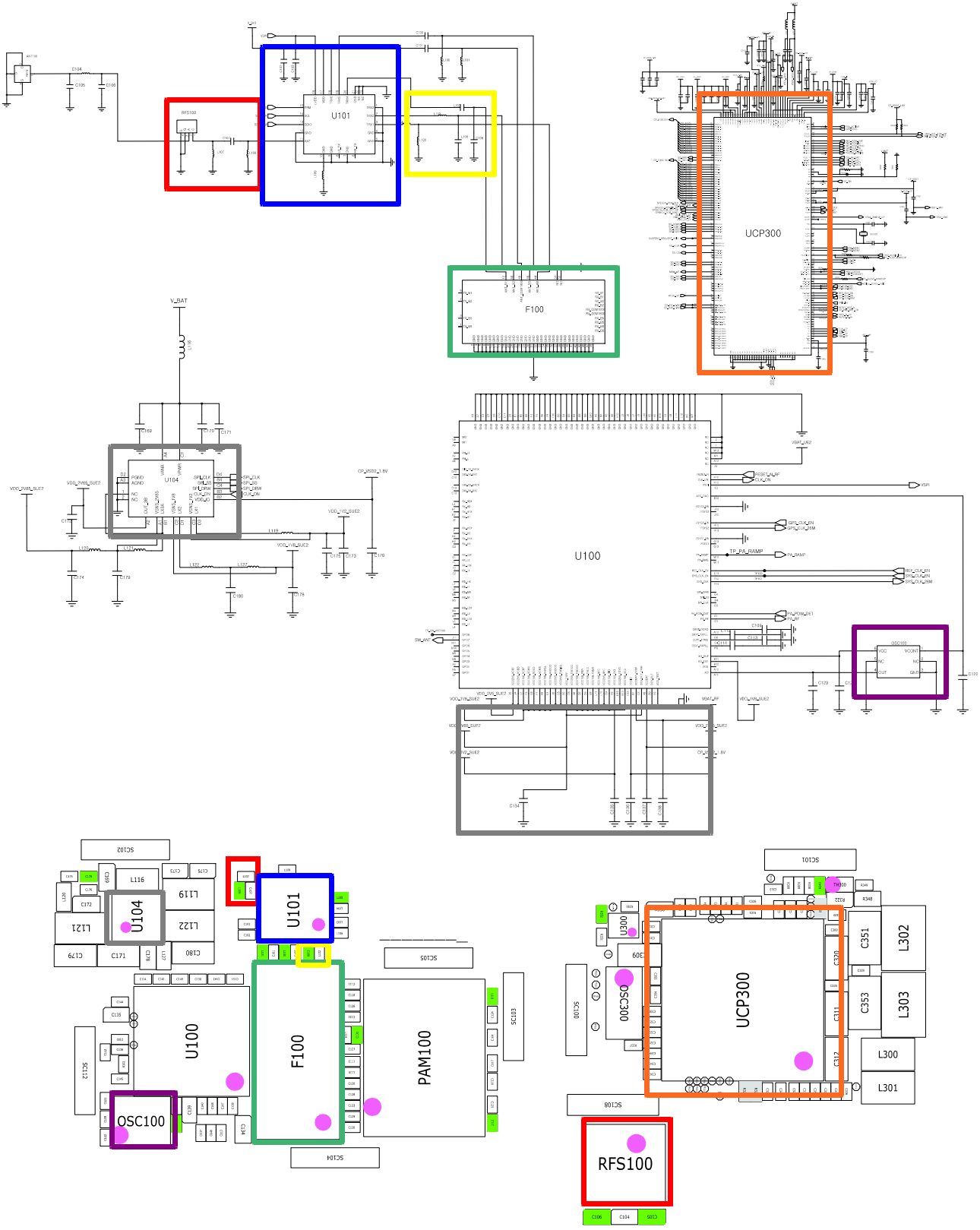

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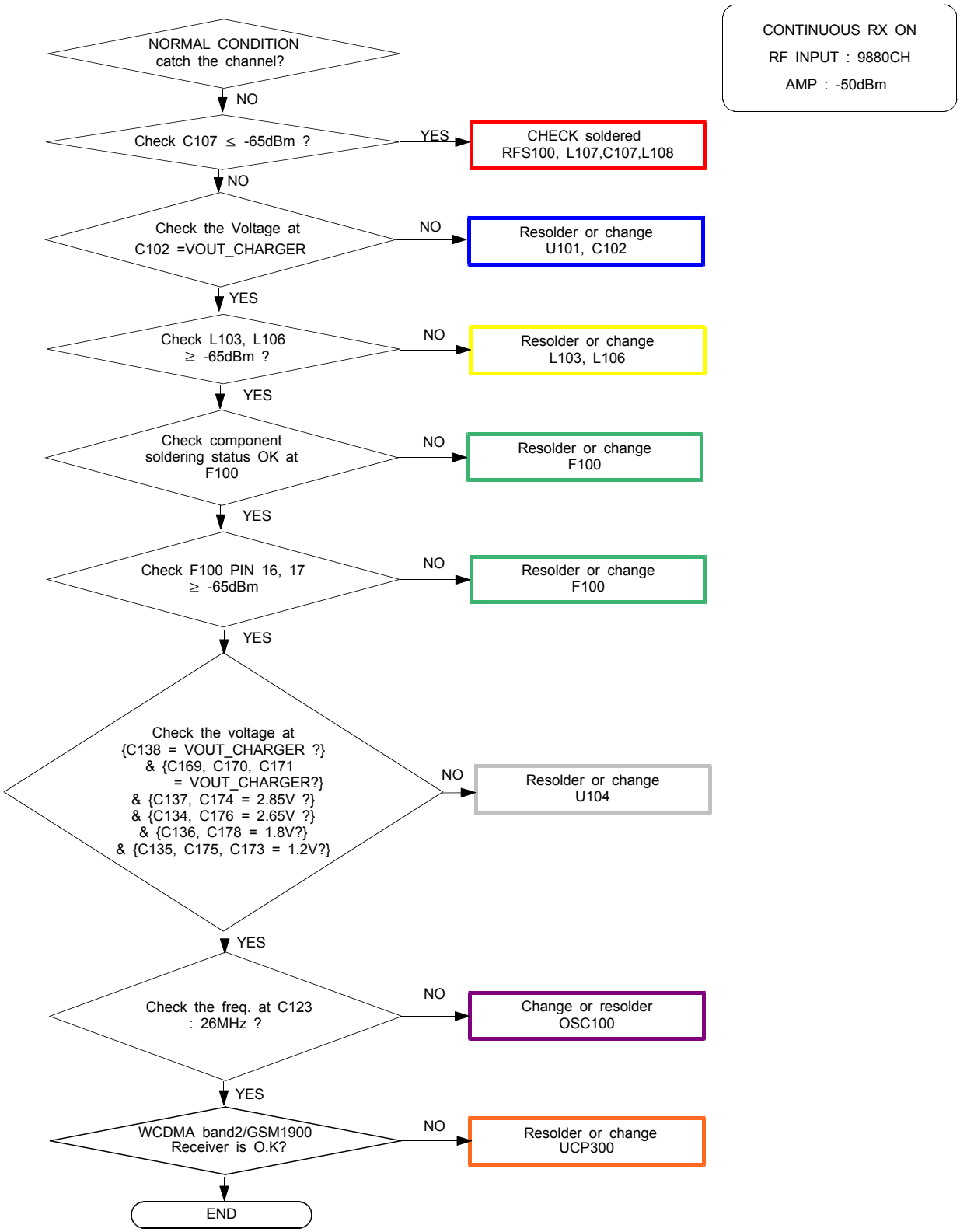
8-3-14. WCDMA Band2 / GSM1900 RX



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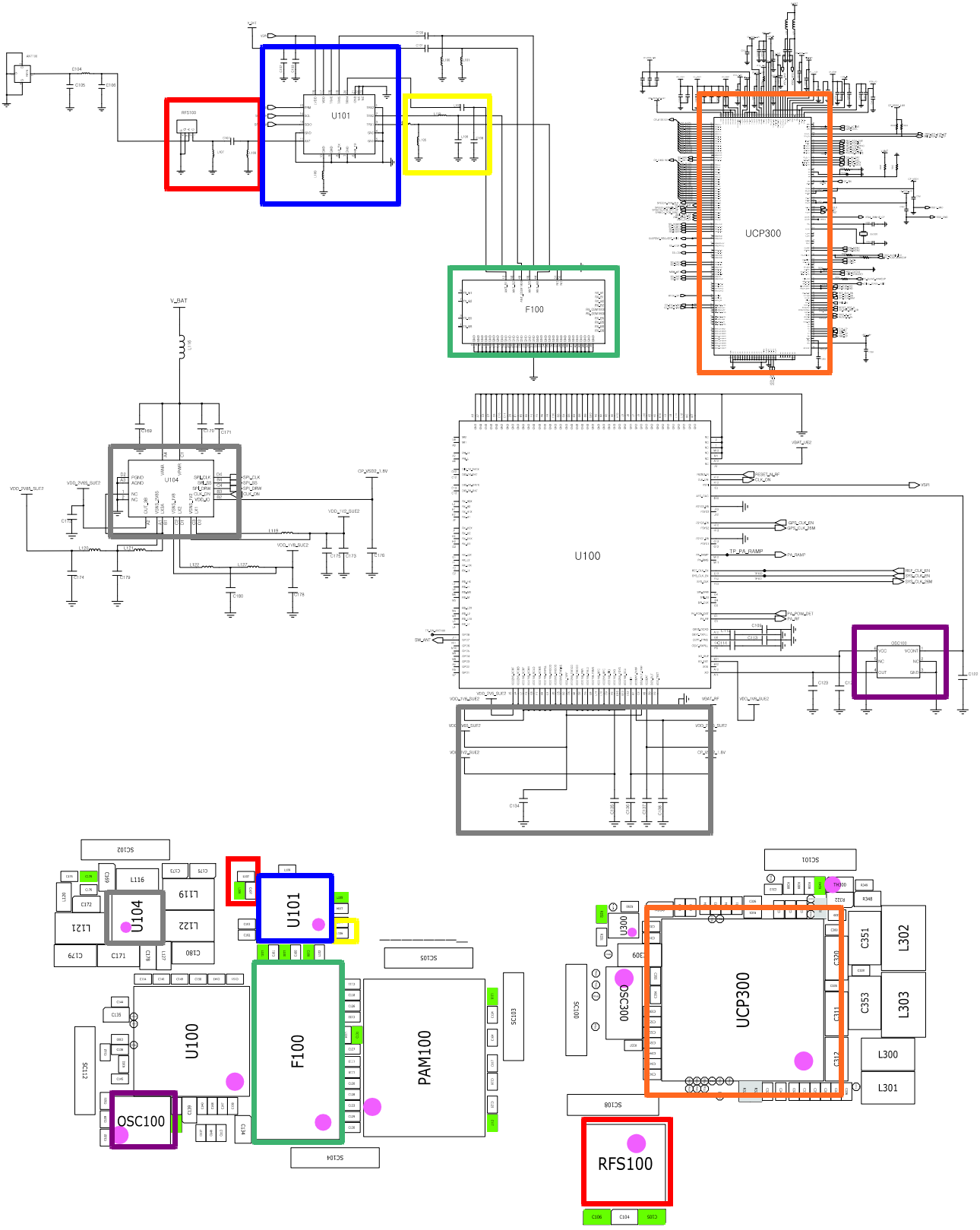

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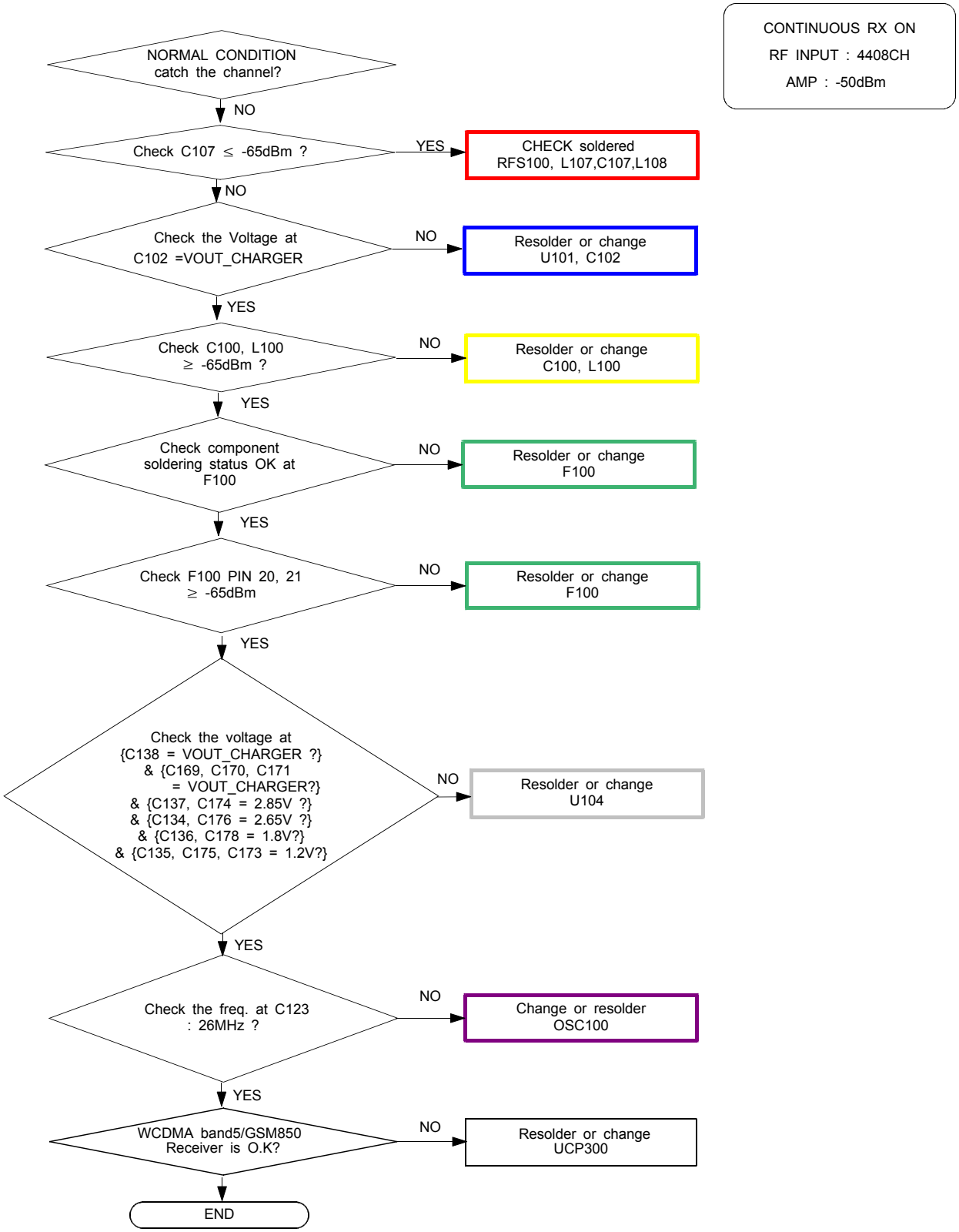
8-3-15. WCDMA Band5 / GSM 850 RX



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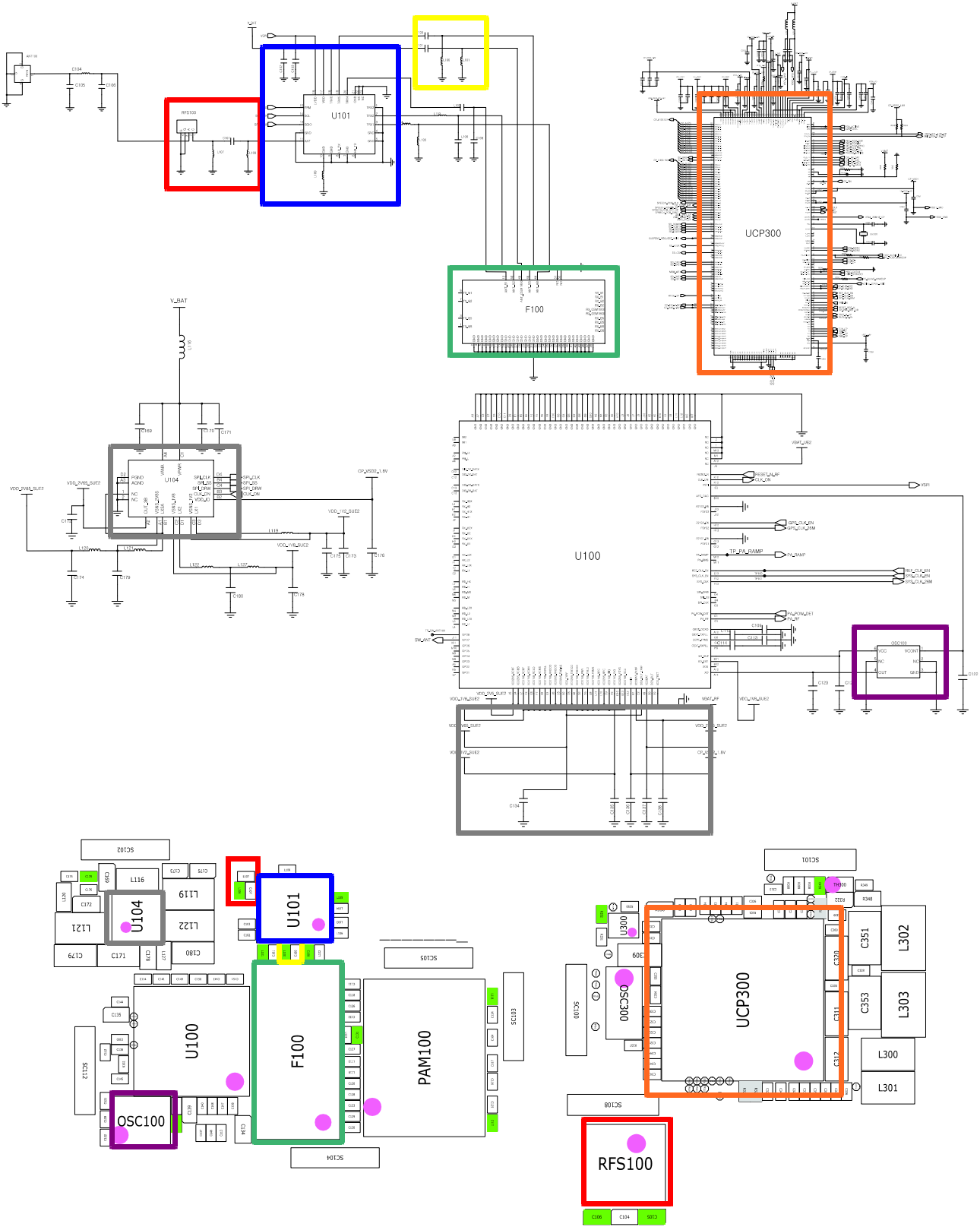

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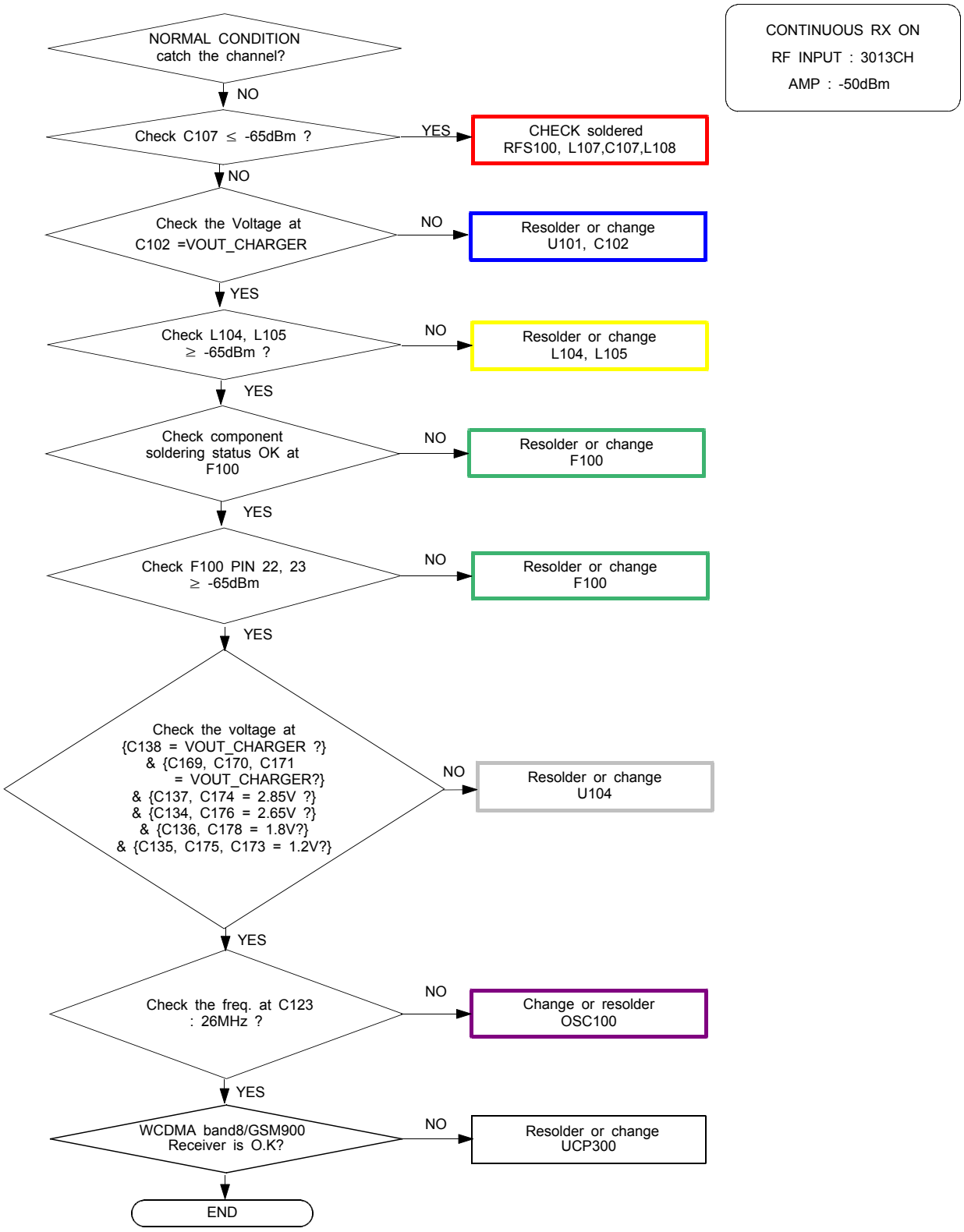
8-3-16. WCDMA Band8 / GSM900 RX



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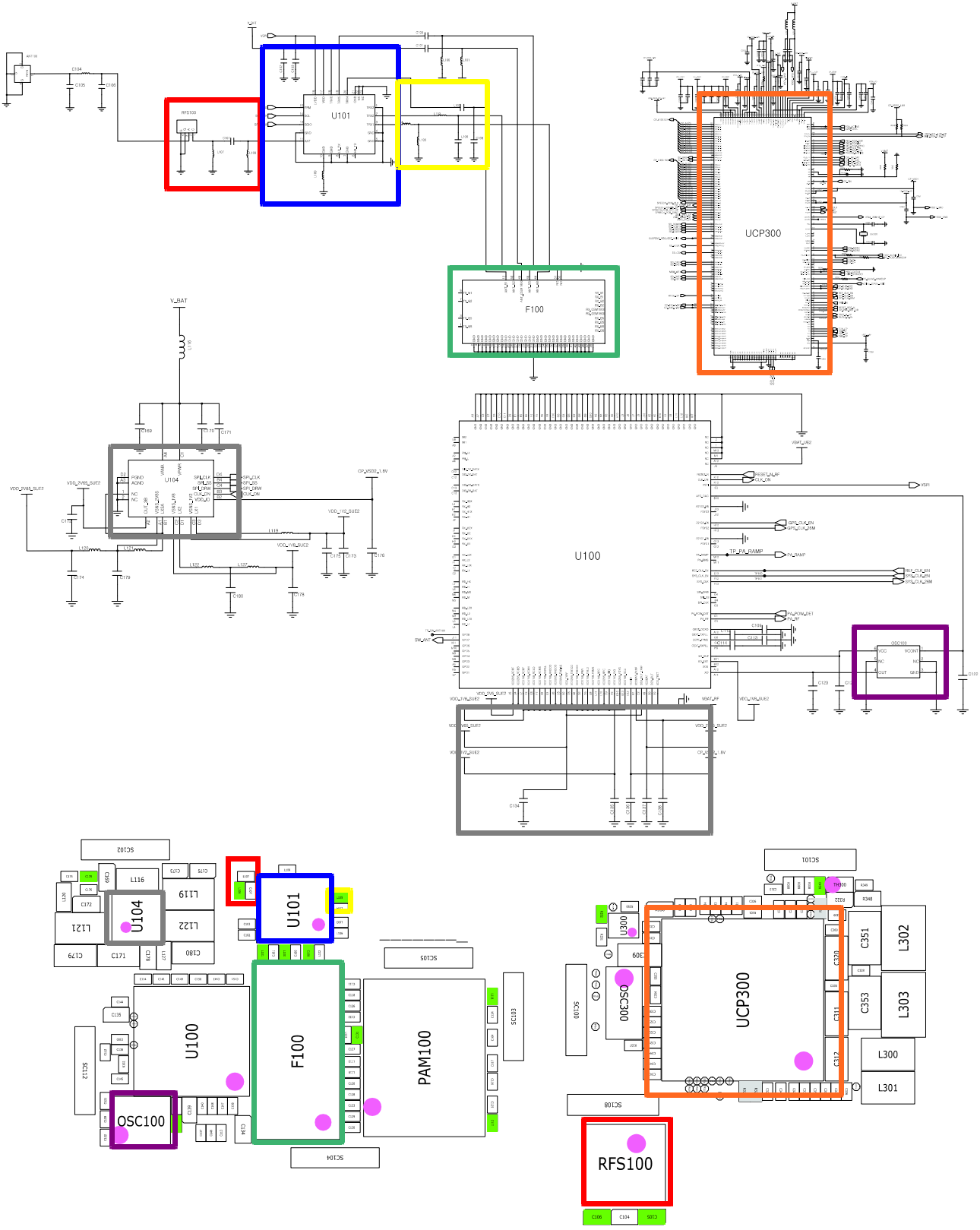

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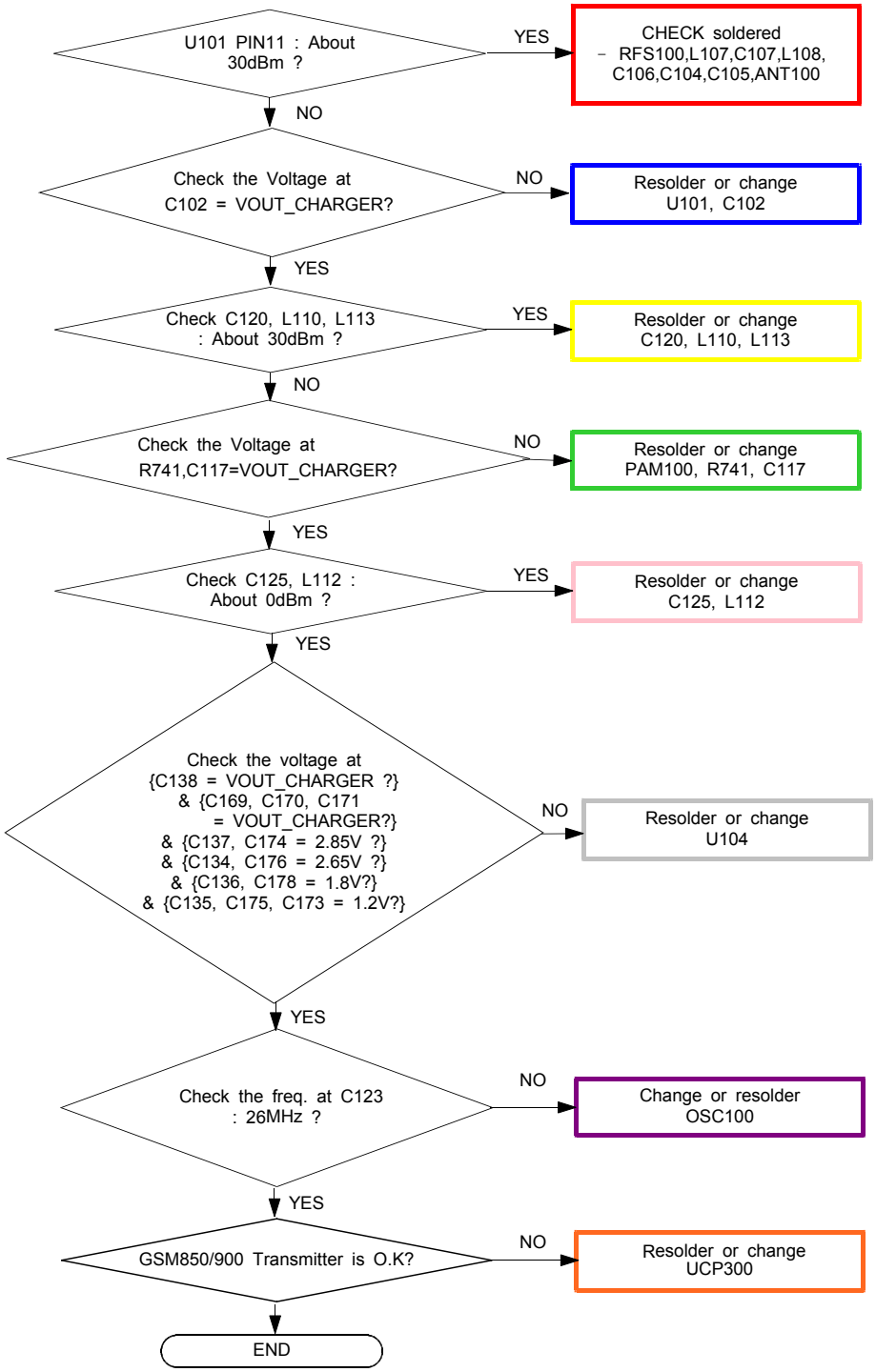
8-3-17. GSM850/GSM900 TX

CONTINOUS TX ON CONDITION
TX POWER DAC:14500 CODE APPLIED
GSM850 CH : 190
GSM900 CH : 62
RBW : 100KHz
VBW : 100KHz
SPAN : 10MHz
REF LEV. : 10dBm
ATT. : 20dB



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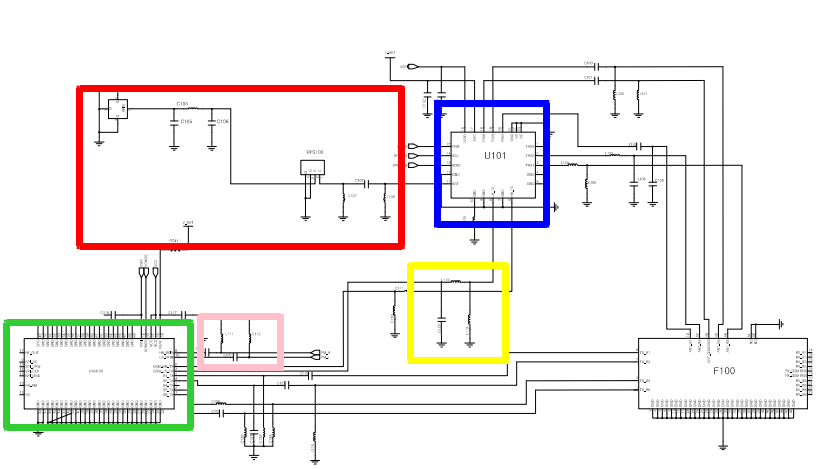

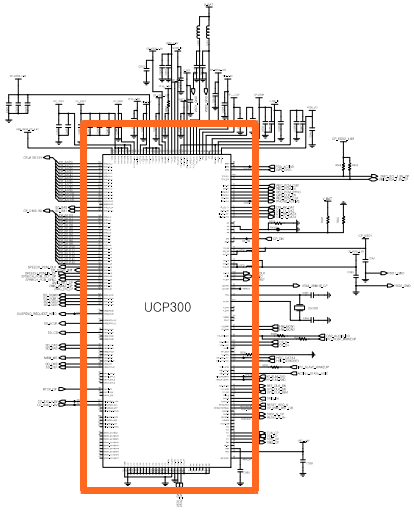

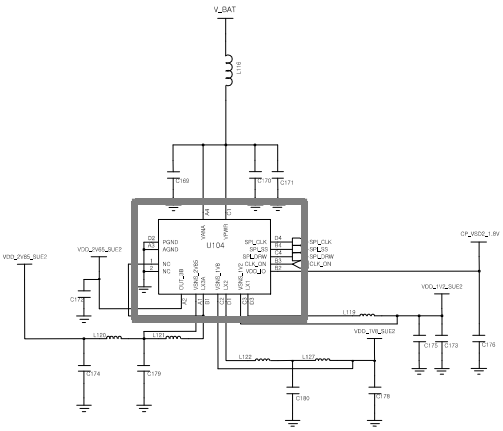

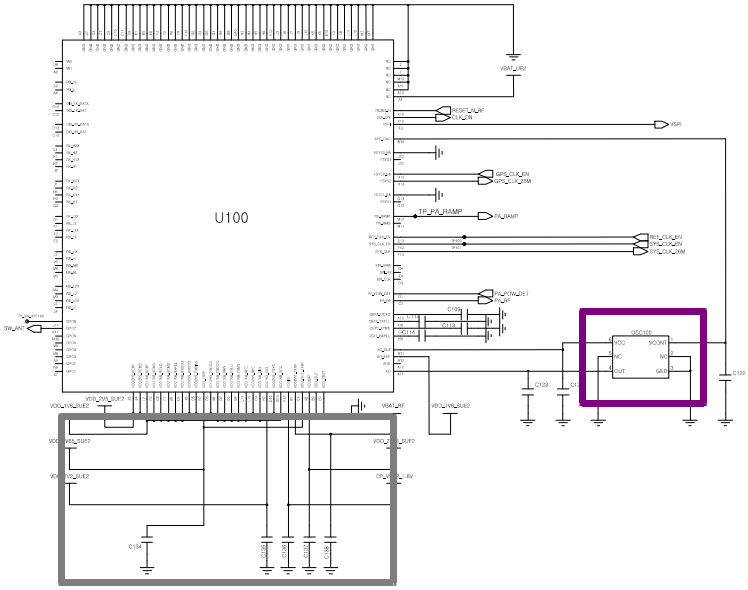

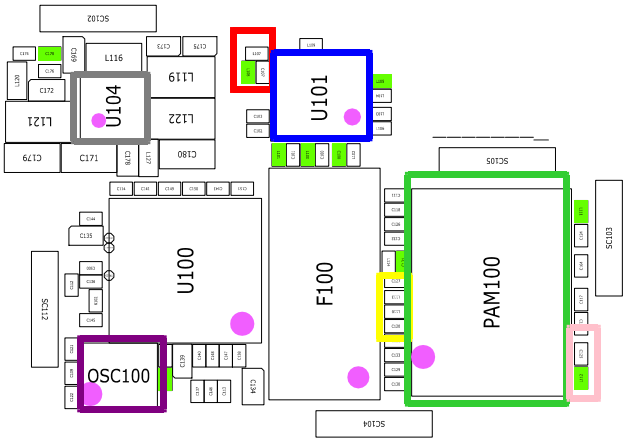

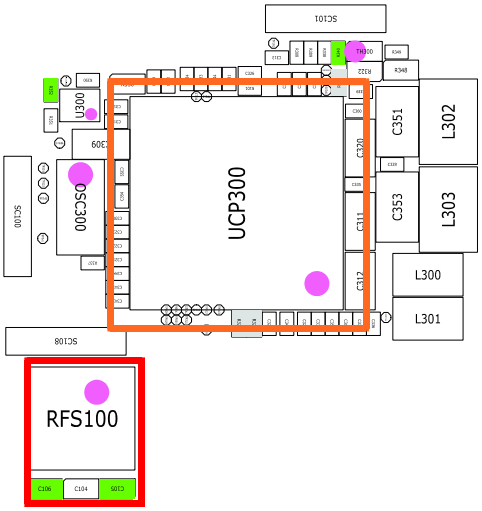

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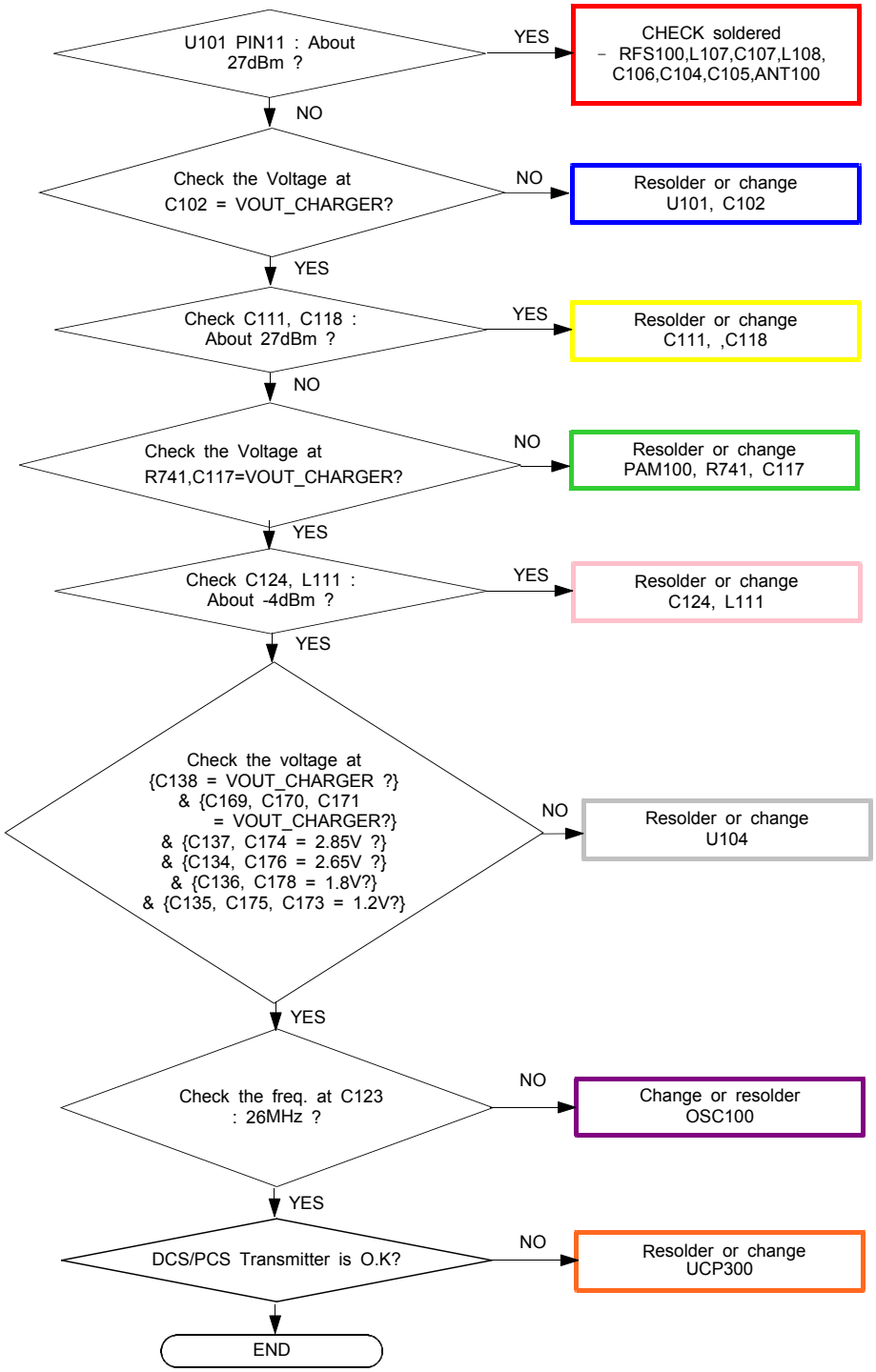
8-3-18. DCS/PCS TX

CONTINOUS TX ON CONDITION
TX POWER DAC:14500 CODE APPLIED
DCS CH : 685
PCS CH : 661
RBW : 100KHz
VBW : 100KHz
SPAN : 10MHz
REF LEV. : 10dBm
ATT. : 20dB



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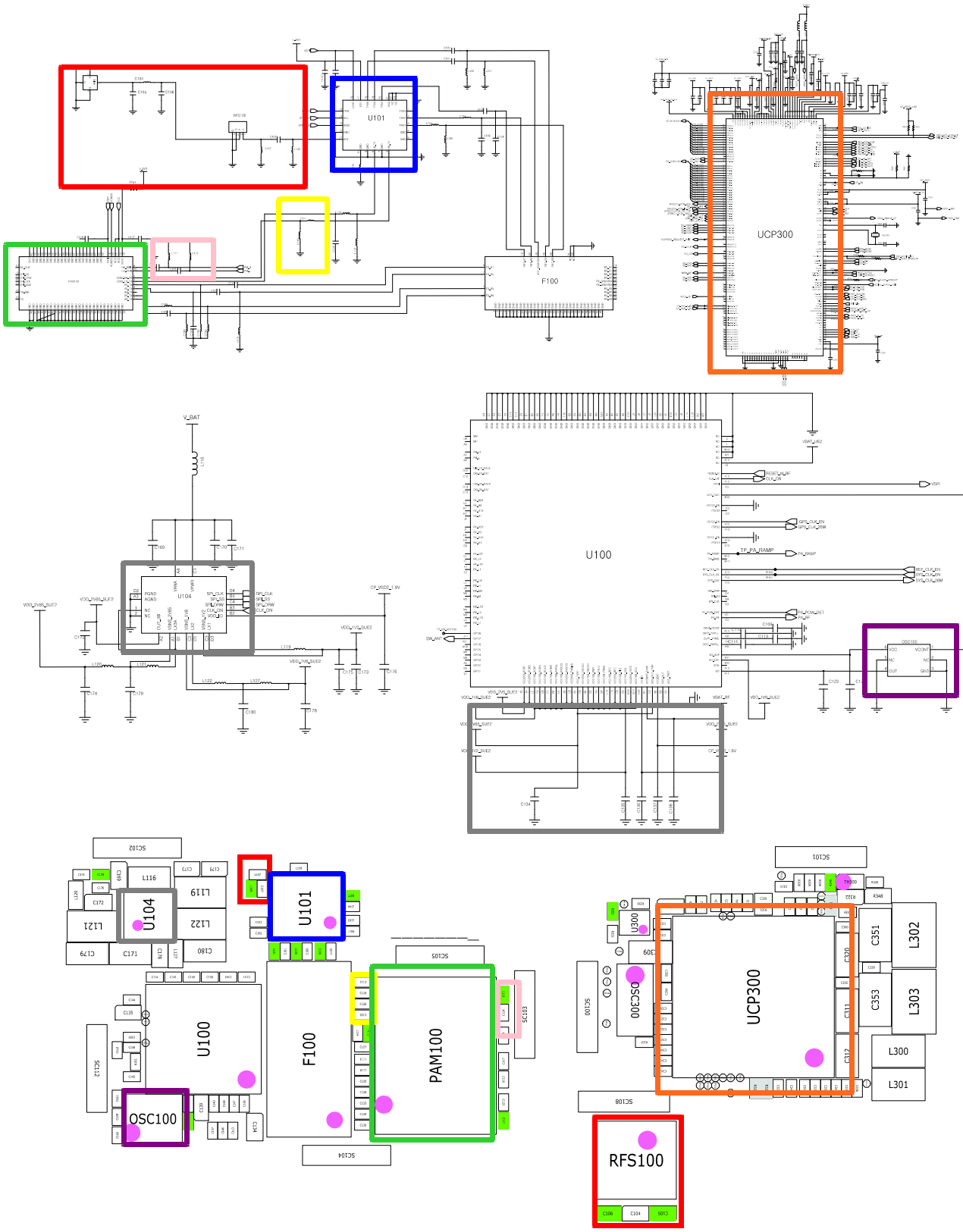

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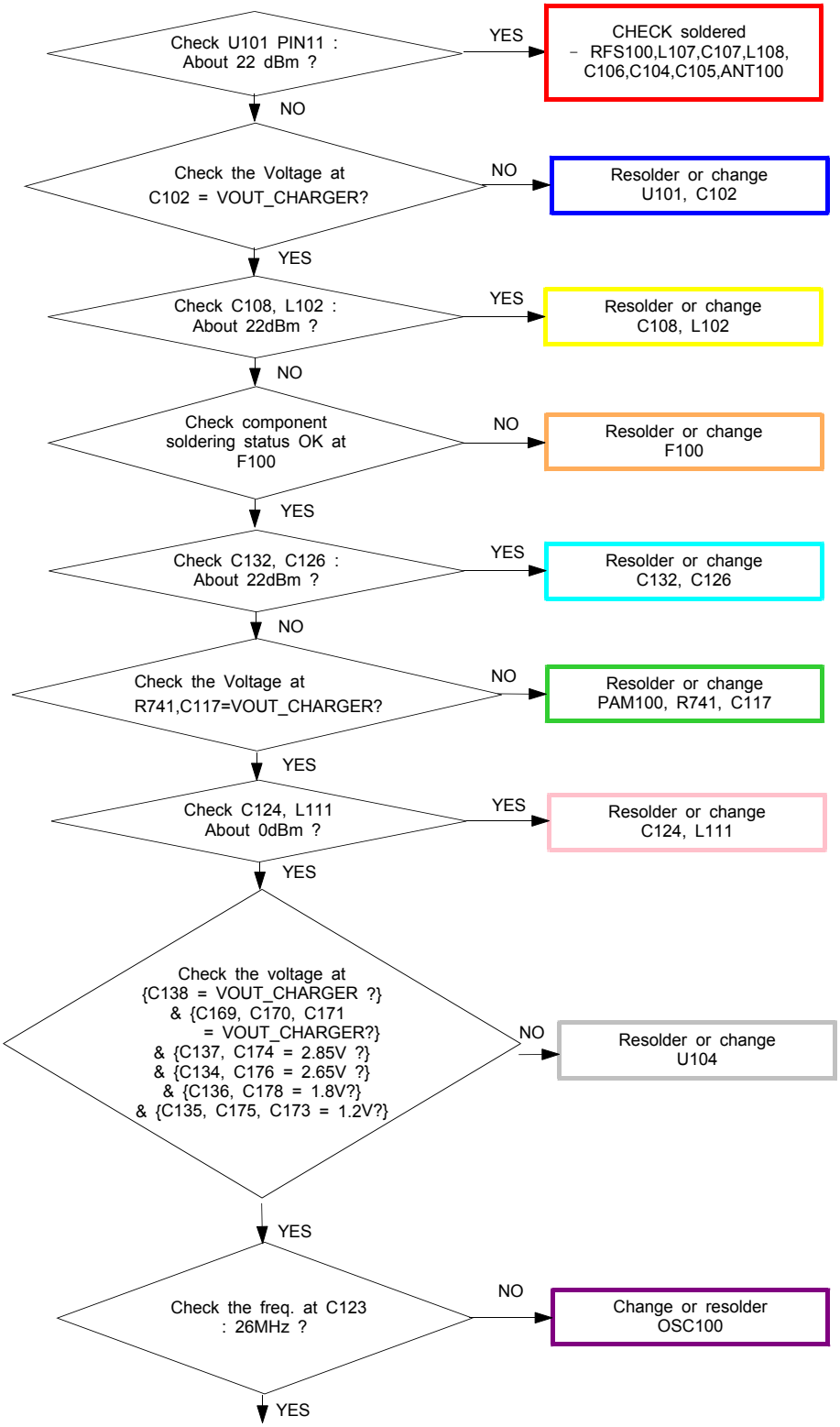
8-3-19. WCDMA BAND1 TX

CONTINOUS TX ON CONDITION
TX POWER DAC:14500 CODE APPLIED
WCDMA Band1 CH : 10700
RBW : 100KHz
VBW : 100KHz
SPAN : 10MHz
REF LEV. : 10dBm
ATT. : 20dB



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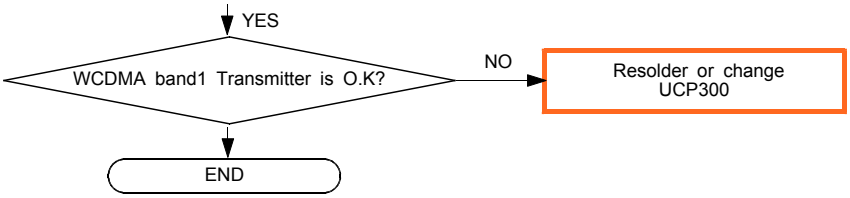

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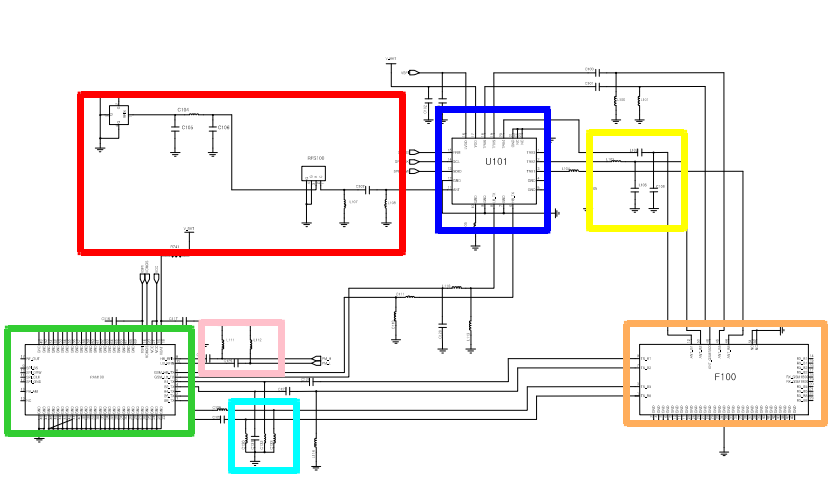

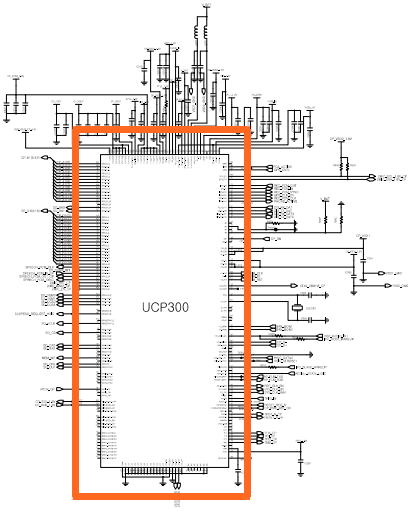

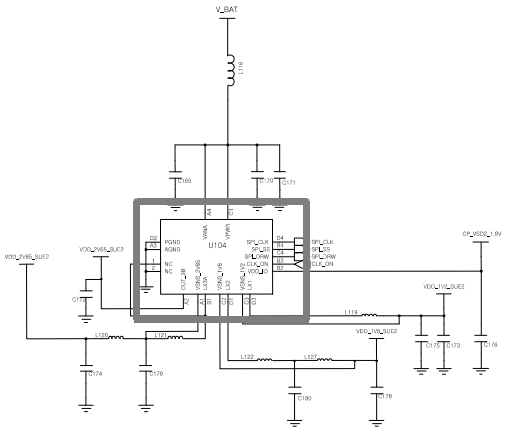

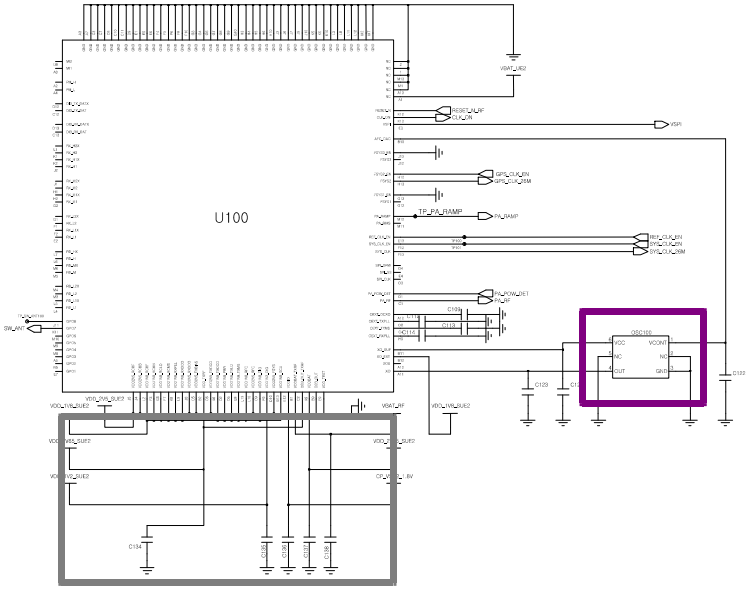

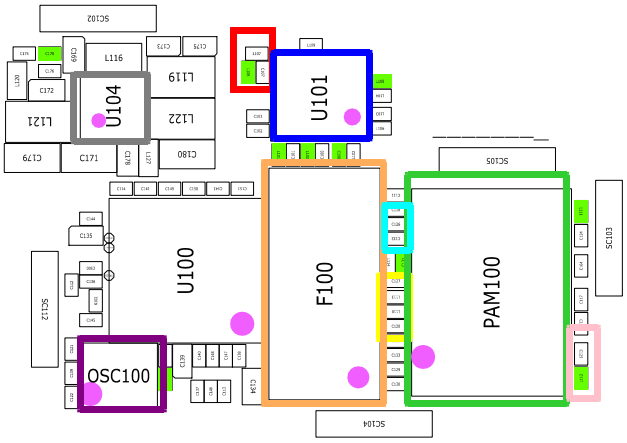

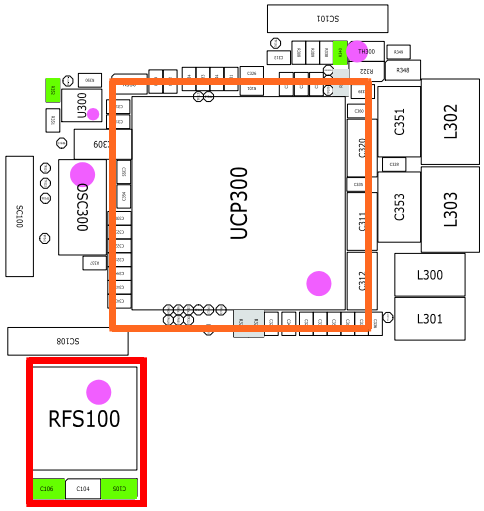

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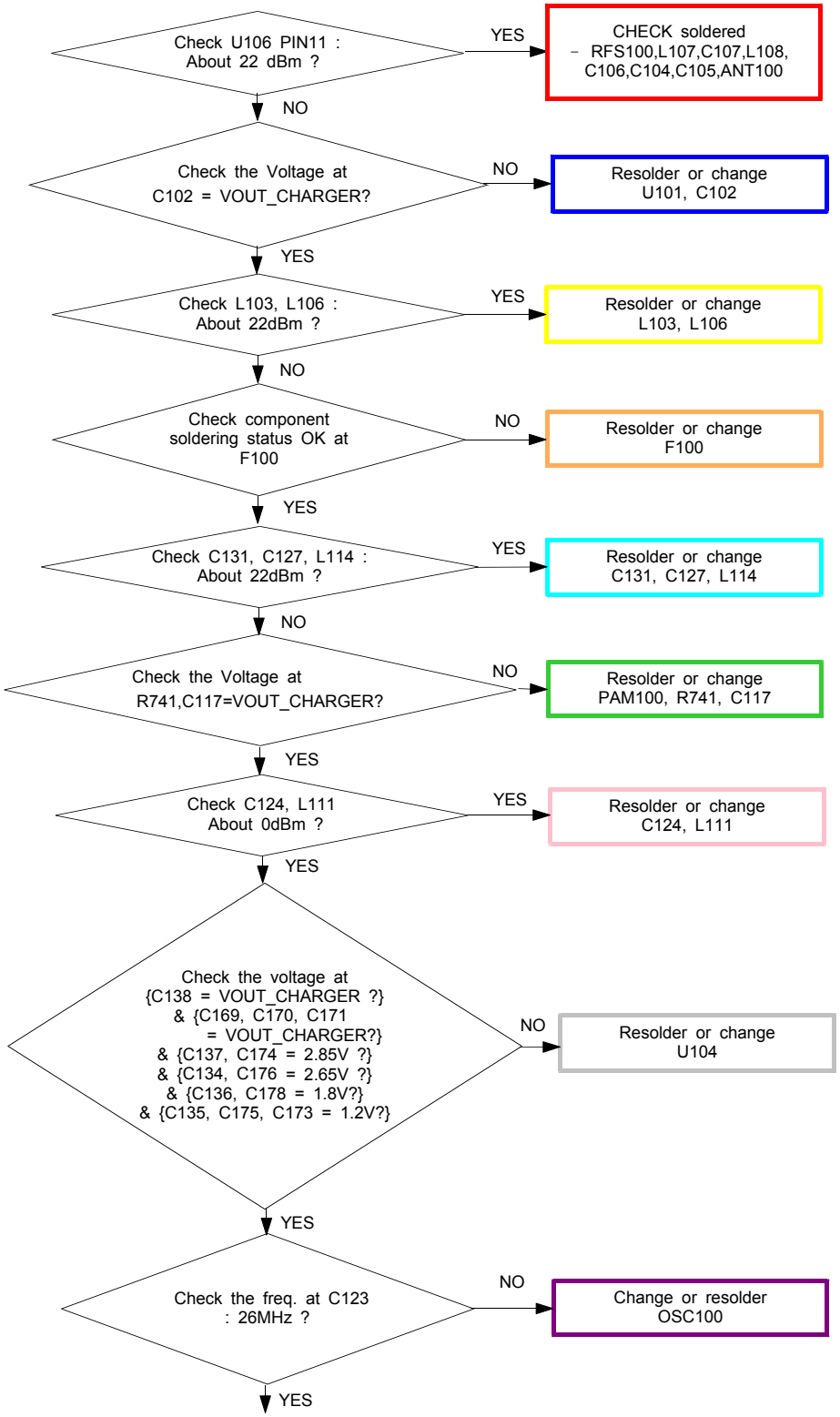
8-3-20. WCDMA BAND2 TX

CONTINOUS TX ON CONDITION
TX POWER DAC:14500 CODE APPLIED
WCDMA Band2 CH : 9880
RBW : 100KHz
VBW : 100KHz
SPAN : 10MHz
REF LEV. : 10dBm
ATT. : 20dB



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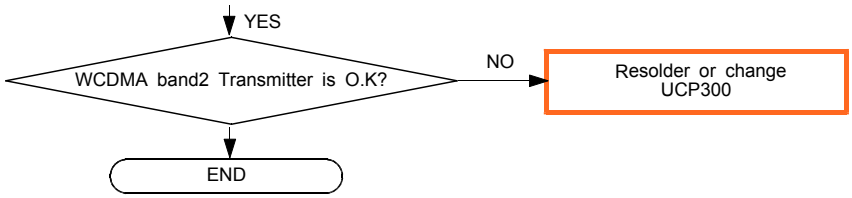

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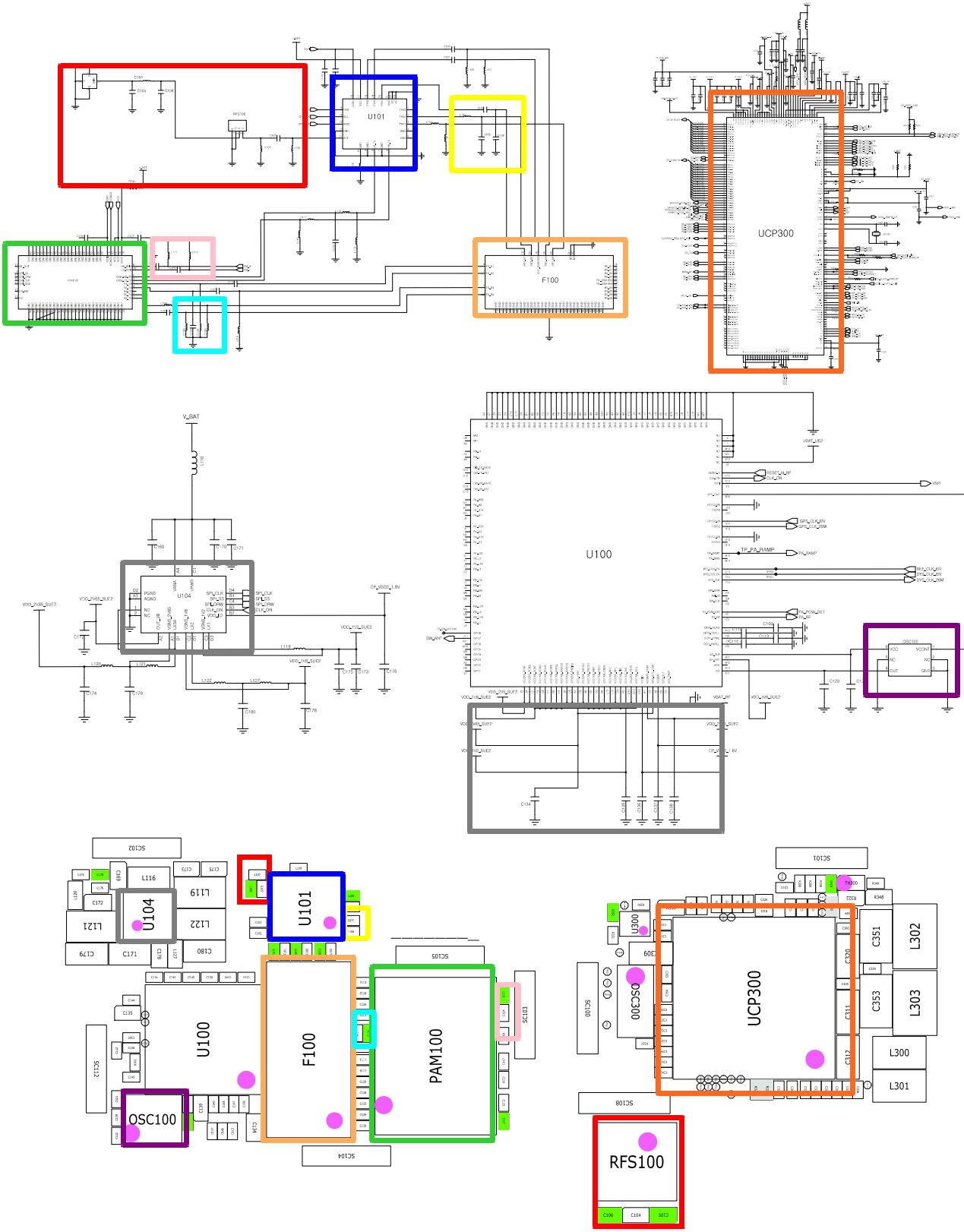

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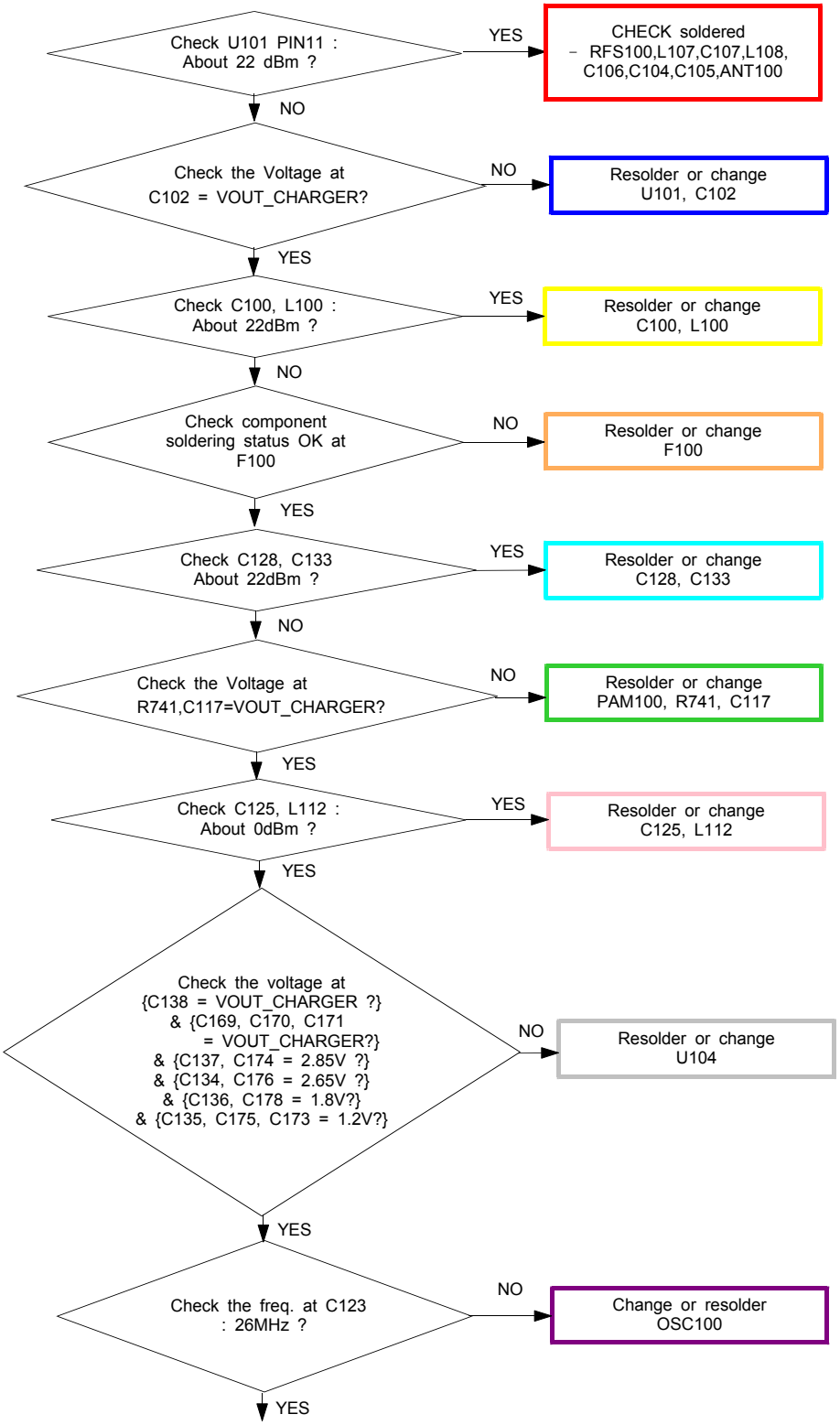
8-3-21. WCDMA BAND5 TX

CONTINOUS TX ON CONDITION
TX POWER DAC:14500 CODE APPLIED
WCDMA Band5 CH : 4408
RBW : 100KHz
VBW : 100KHz
SPAN : 10MHz
REF LEV. : 10dBm
ATT. : 20dB



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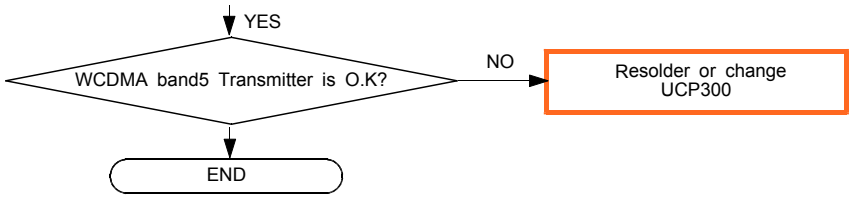

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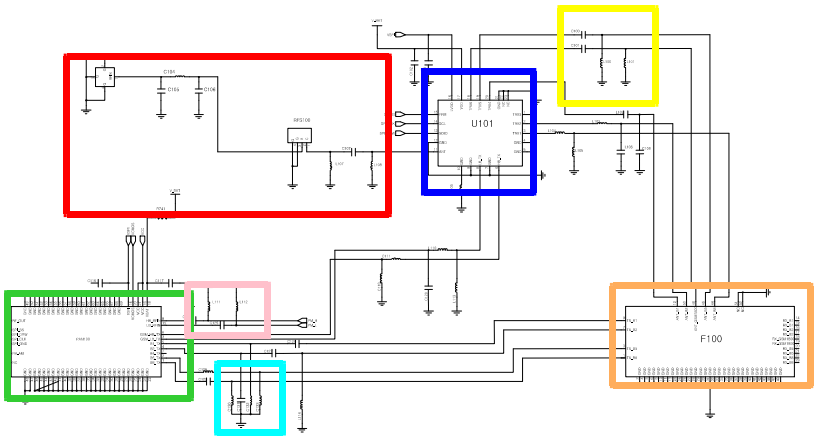

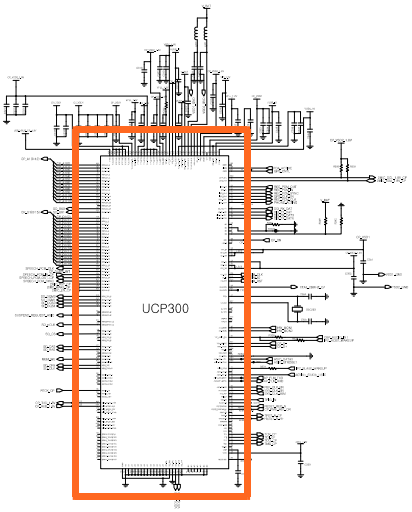

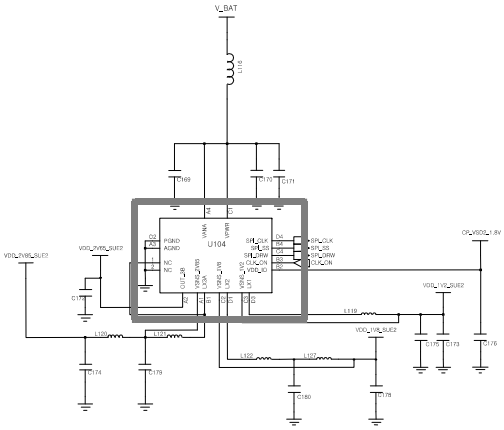

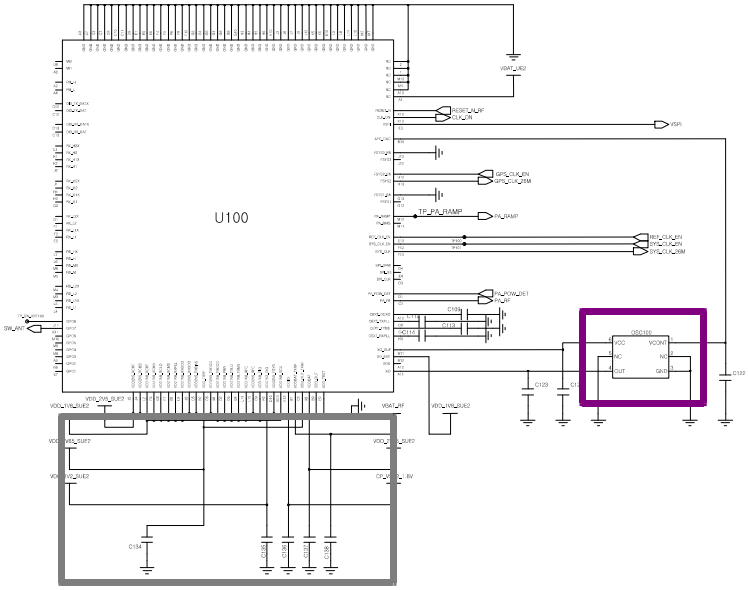

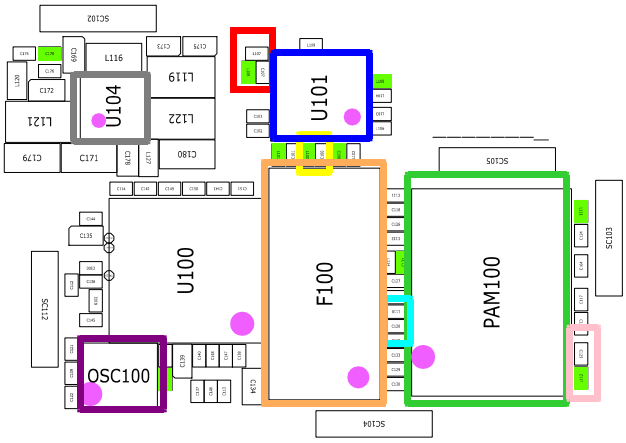

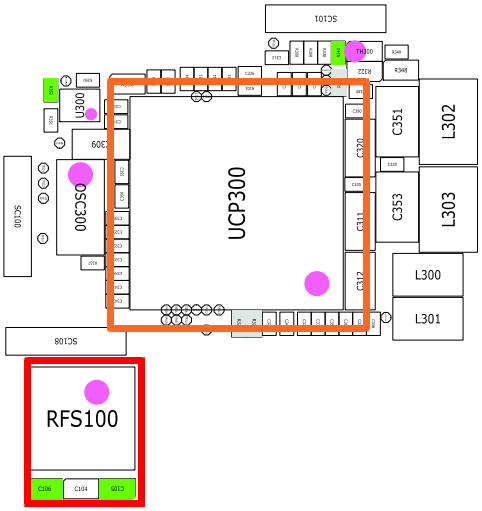

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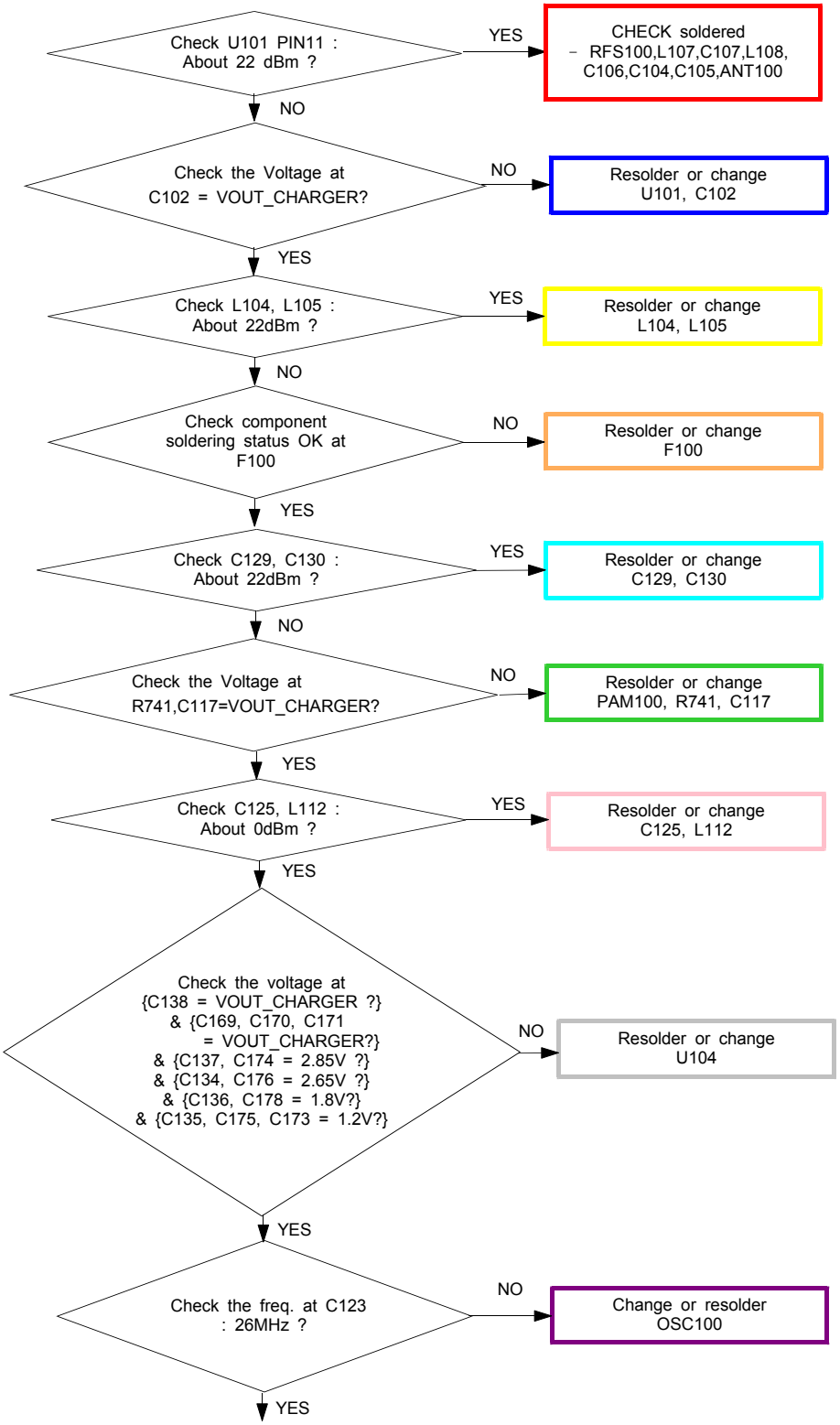
8-3-22. WCDMA BAND8 TX

CONTINOUS TX ON CONDITION
TX POWER DAC:14500 CODE APPLIED
WCDMA Band2 CH : 3013
RBW : 100KHz
VBW : 100KHz
SPAN : 10MHz
REF LEV. : 10dBm
ATT. : 20dB



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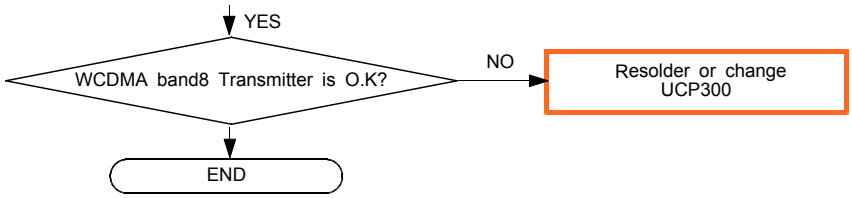

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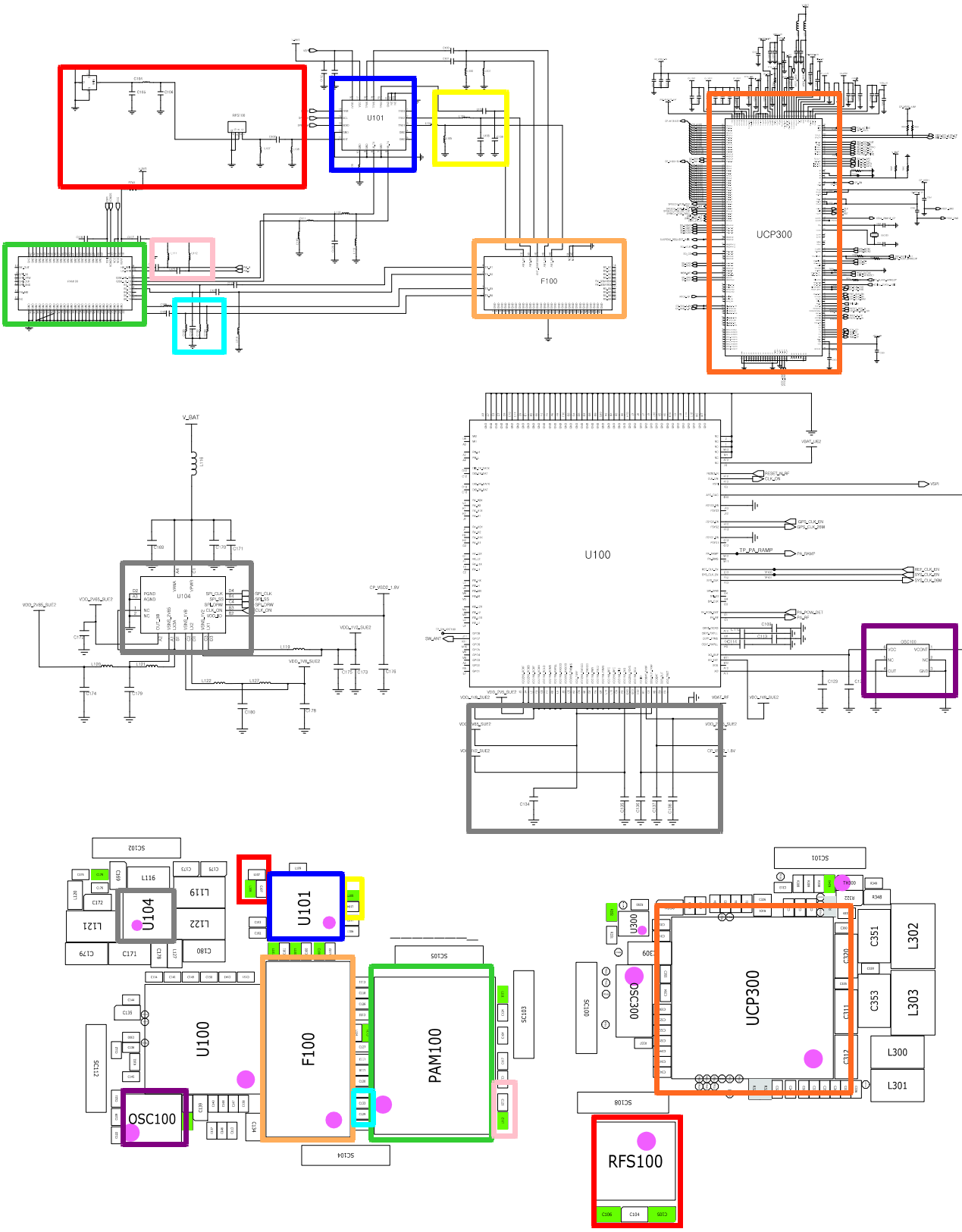

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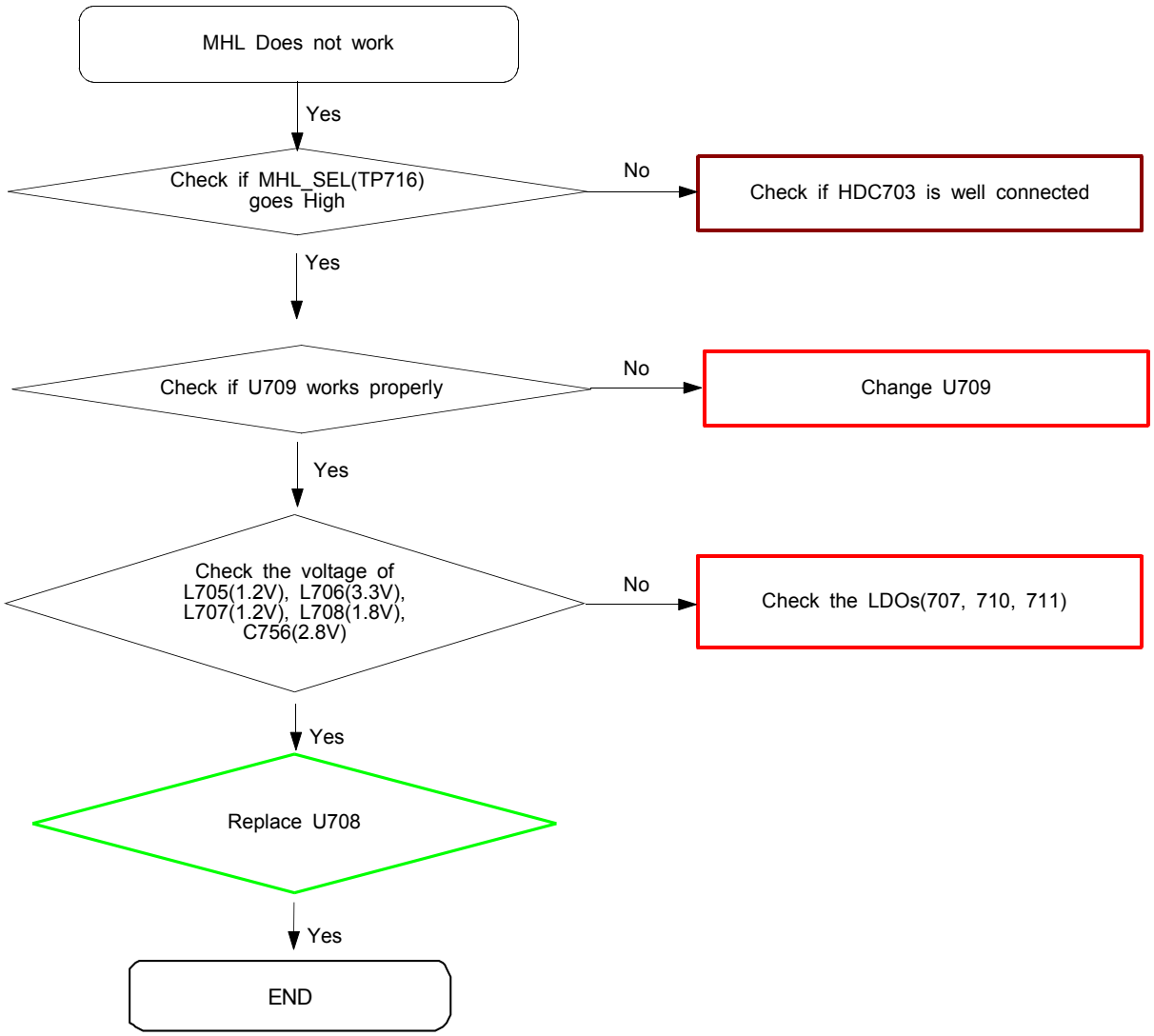
8-3-8. MHL



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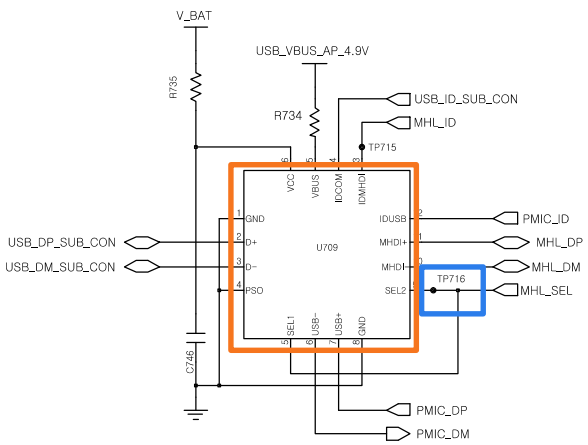
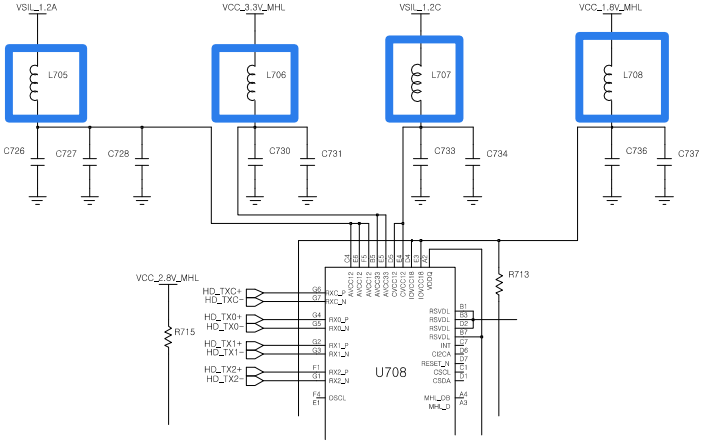
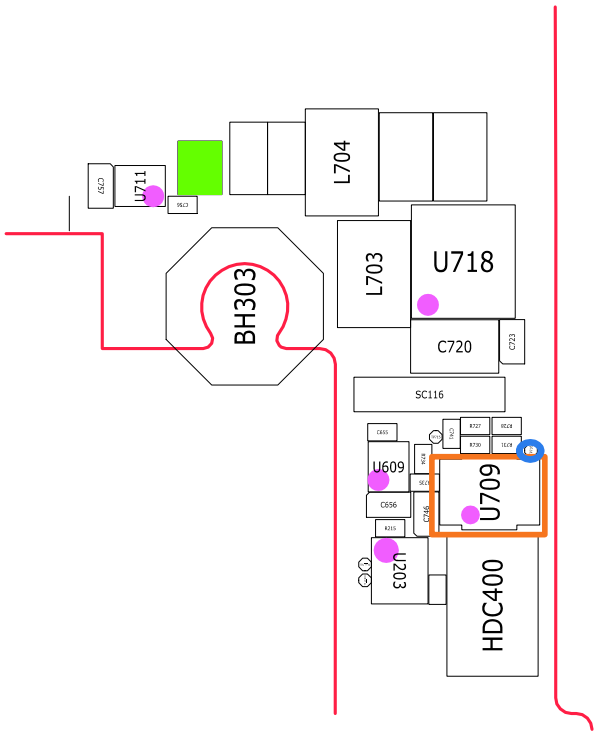
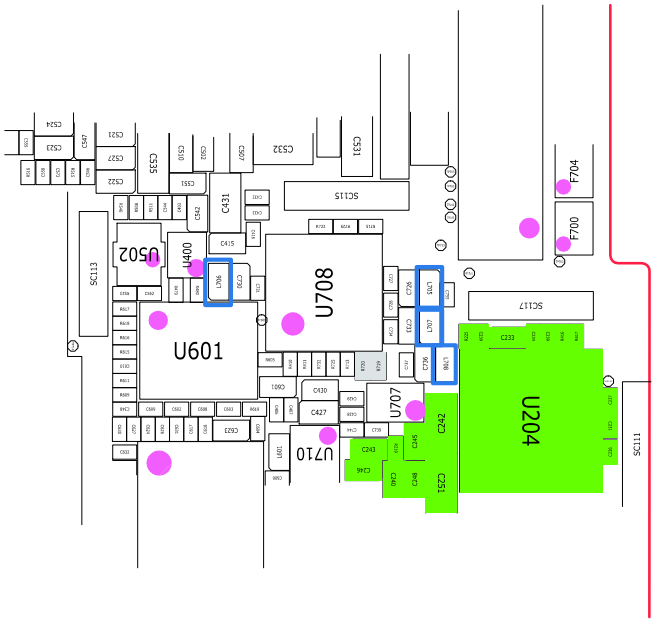
8-3-8. MHL









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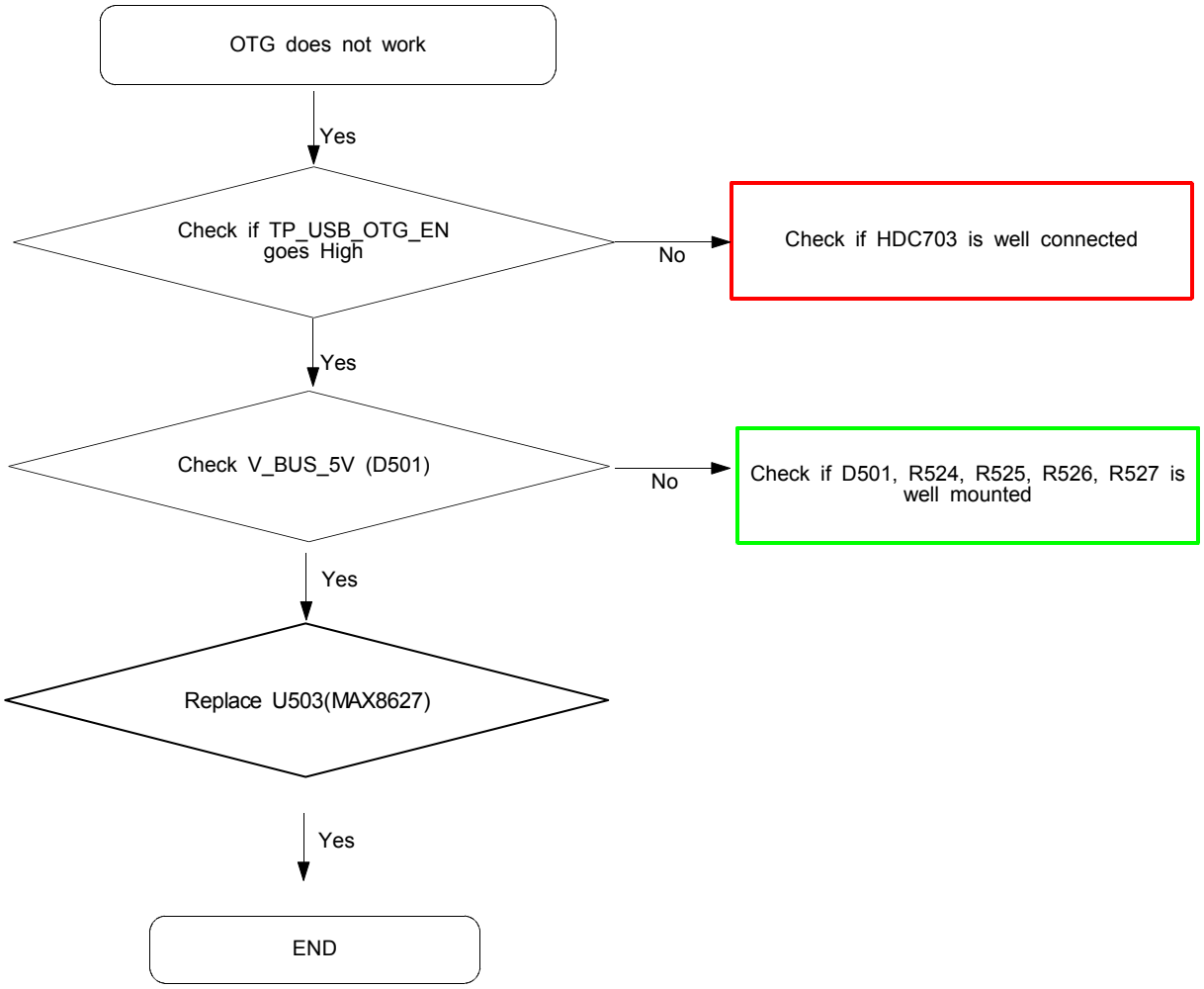
8-3-9. OTG



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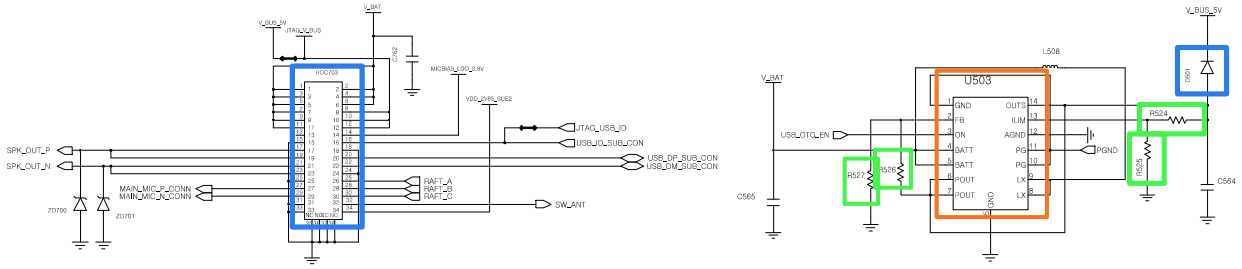
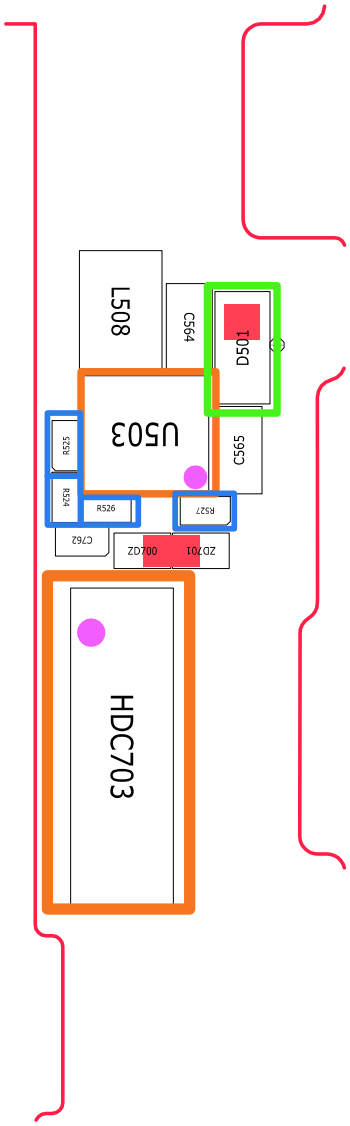
8-3-9. OTG





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8-4. Service Schematics

- NC Point(Top View)

UCP400

: **NC**

2.1 Pin Assignment Diagram

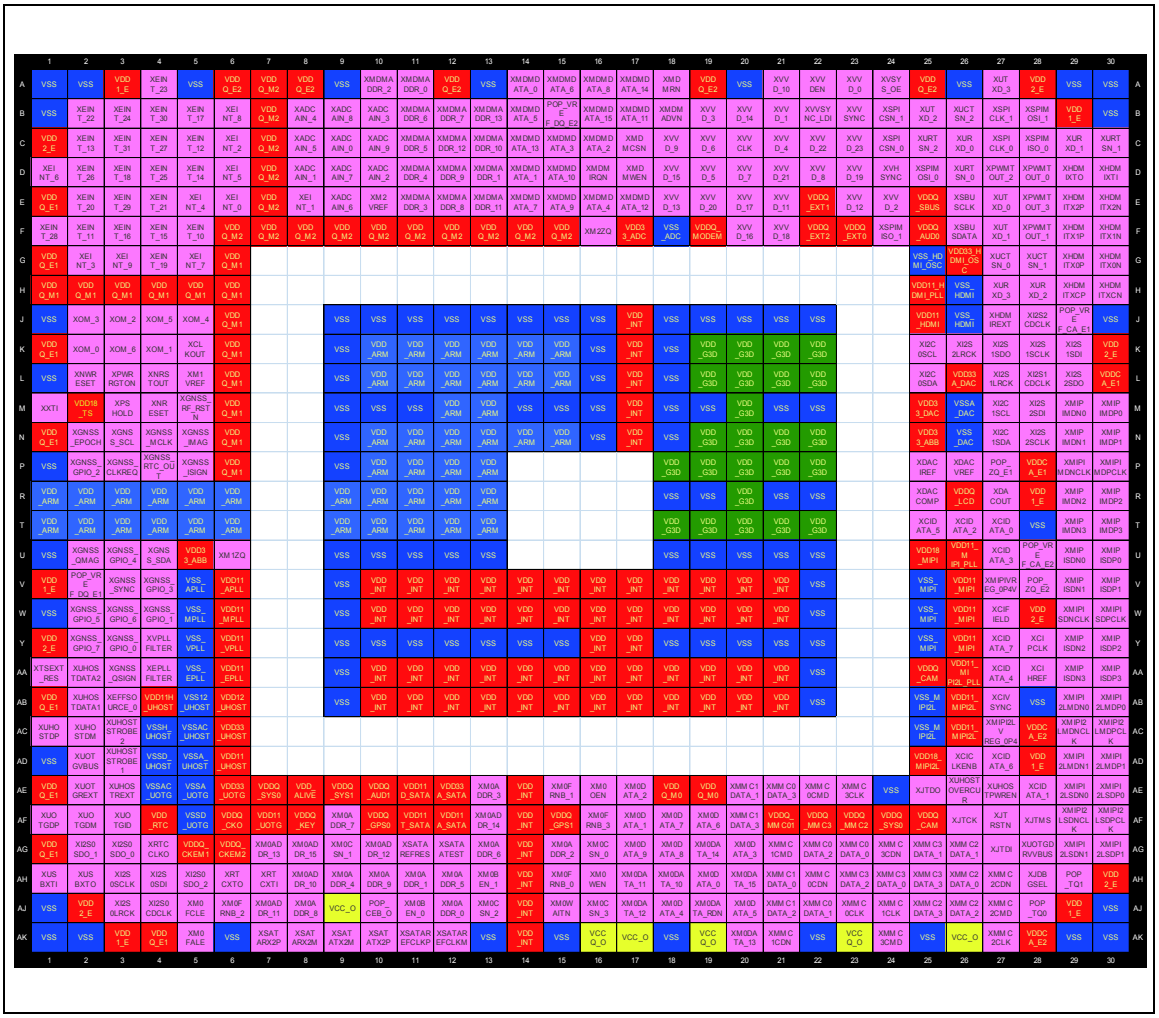

Figure 2-1 S5PC210 Pin Map(756-FCMSP) Top View

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UCP300

XG626 Ball Map (Bottom View) 6 /15/2010 7.5x7.5 FBGA

	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	NC	MEM_A_8	MEM_BFCLKO_1	MEM_SDCLKO	MEM_A_0	MEM_BC0_n	MEM_A_1	MEM_A_2	MEM_A_3	MEM_A_4	MEM_AD_9	FCDP_RBn	VPLL	VDD_VBAT_SD2	SD2_SW	SD2_SW	NC	A
B	MEM_A_9	MEM_A_23	MEM_BFCLKO_0	MEM_CKE	MEM_RD_n	MEM_WR_n	VDD_IO18	MEM_BC2_n	MEM_A_6	FWP	MEM_CAS_n	DSP_AUDIO_IN1	x	VIO_12	x	x	VSS_SD2	B
C	MEM_A_10	MEM_A_22	xx		x	MEM_A_5	x	x	MEM_A_7	x	x	x	x	VUSB_PD	VDD_VSD2	SD2_FB	VDD_VBAT_SD1	C
D	MEM_A_11	MEM_A_21	x	VSS	MEM_AD_13	MEM_AD_12	MEM_AD_11	MEM_AD_7	VSS	MEM_AD_3	x	x	x	ANAMON	SD1_FB	x	SD1_SW	D
E	MEM_A_12	MEM_A_20	x	MEM_RAS_n	VDDCORE	VDDCORE_EBU	MEM_AD_8	VDDCORE	MEM_AD_6	MEM_AD_5	x	x	x	VSS	FSS	x	SD1_SW	E
F	MEM_A_13	MEM_BC1_n	VDD_IO18	VSS	MEM_AD_15	xx		x	MEM_AD_4	x	x	TRIG_B	x	VRTC	VDD_VBAT_PMU	VUSB_ANA	VSS_SD1	F
G	MEM_A_14	MEM_BC3_n	MEM_A_19	MEM_BE0_n	MEM_BE1_n	x	MEM_AD_1	MEM_ADV_n	MEM_AD_2	VSS	x	xxx			x	VPMU	VSIM	G
H	MEM_A_15	MEM_A_17	x	MEM_CS2_n	MEM_CS3_n	x	MEM_AD_0	MEM_AD_10	VDDCORE	RESERVED	x	M1	x	x	AGND	ON1	VUSB_IO	H
J	VDD_IO18	MEM_A_16	MEM_A_18	MEM_CS0_n	MEM_CS1_n	MEM_AD_14	VSS	x	x	VSS	x	M2	M3	M4	RESET_PWRDWN_N	ON2_N	VREF	J
K	MEM_WAIT_n	VDD_MIPI	x	VDDCORE	VSS	x	VDD_IO18	EINT3	VDDCORE	VDD_IO18	ETM11_TRACECLK	x	ETM11_TRACEPKT4	TM_EN	REF_CLK_EN	RESET_BB_N	ETM11_TRACEPKT7	K
L	F32K	VSS	x	VSS	MIPI_HSI_RX_RDY	x	MIPI_HSI_TX_FLG	VSS	ETM11_TRACEPKT5	VDD_MMC	MMCI1_CMD	x	ETM11_TRACEPKT6	ETM11_TRACEPKT2	x	ETM11_TRACEPKT3	ETM11_TRACEPKT1	L
M	OSC32K	VSS	MIPI_HSI_TX_RDY	MIPI_HSI_RX_FLG	MIPI_HSI_TX_WAKE	xx		x	EINT1	EINT2	x	MMCI1_DAT_3	MMCI1_DAT_0	MMCI1_DAT_2	MMCI1_CLK	MMCI1_DAT_1	ETM11_TRACEPKT0	M
N	VDD_RTC	USB_ID	x	VSS_USB	MIPI_HSI_RX_DATA	MIPI_HSI_TX_DATA	VDD_IO18	I2C1_SCL	VPP	CLKOUT0	x	x	MMCI1_CD	T_OUT0	x	I2S2_CLK1	I2S2_CLK0	N
P	USB_TEST	VBUS	x	VDD_USB_ANA	MIPI_HSI_RX_WAKE	SYS_CLK	VSS_PLL	CLKOUT2	I2C1_SDA	VSS	HW_MON2	xx		x	T_OUT1	I2S2_TX	I2S2_RX	P
R	USB_DMINUS	VDD_USBIO	xx		x	VDD_PLL	x	x	VSS	VDDCORE	x	HW_MON1	RESET2_N	NC	x	I2S2_WA1	I2S2_WA0	R
T	USB_DPLUS	USB_TUNE	VDD_USB_PD	CC_RST	CC_IO	VDD_SIM	DMINUS	VDD_DIG_RF	XRESET_N	Di3_TX_DATX	Di3_TX_DAT	TCK	TRIG_IN	TRST_n	USIF1_TXD_MTSR	USIF1_RXD_MRST	USIF1_SCLK	T
U	NC	VSS	VDD_IO12	CC_CLK	HSIC_USB_DATA	HSIC_USB_STRB	DPLUS	ALERT_N	SYSCLKEN	Di3_RX_DATX	Di3_RX_DAT	TMS	TDI	TDO	USIF1_RTS_N	USIF1_CTS_N	NC	U
	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

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U501

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	NC	FLED 2	FLED 1	OUTF	LXF	PGN DF	PGN D6	LX6	INB 06A	GND M	IN_ MOTOR	INB 02	NC
B	FGND	FGND	D GND2	OUTF	LXF	PGND F	PGN D6	LX6	INB 06B	MDN	MDP	BUCK 2	LX2
C	XIN	XOUT	32kHz AP	32kHz CP	FLED _EN	GSMB	REF INPA	BUCK 6EN	BUCK 6	M PWM	M GAIN	PGN D2	PGN D3
D	VL	SAFE OUT1	SAFE OUT2	VCC_ 32CP	COMP	RSO\	IRQ1\	MR2\	MR1\	IN_ GPIO2	IN_ GPIO1	BUCK 3	LX3
E	BATT	BATT	DET BAT\	V COIN	PWR ON	JIG ON	SCL	GPIO 7	GPIO 6	GPIO 1	GPIO 0	INB 03	INB 07
F	DCIN	DCIN	VICH G	18 VLL	PWR HOLD	ONO\	SDA	GPIO 9	GPIO 8	GPIO 3	GPIO 2	BUCK 7	LX7
G	DN1	BC	18T NC2	28T1	18R NC1	CB	SET3	GPIO 11	GPIO 10	GPIO 5	GPIO 4	PGN D 7	PGN D 7
H	DP2	SL1	UT1	28T NO2	28T COM1	28R NO1	SET2	SET1	PWR EN	GPIO _GND	D GND1	A GND	GND
J	COM N1	SR2	UR2	18R1	VBAT TFG	THRM	AIN	VTT	LDO 13	LDO 12	LDO 11	LDO 17	LDO 9
K	COM P2	MIC_ USB	18T2	28R COM2	ALRT	VBFG	SCA FG	LDO 21	INL 21	LDO 18	LDO 14	LDO 16	LDO 15
L	UID	IDB	BOOT	28R2	SDA FG	KVSS	SNS	LDO 2	LDO 10	INL 4	INL 3	INL 2	INL 1
M	PGN D 5	BUCK 5	INB 05	BUCK 4	BUCK 1	PGN D 1	LX1	INB 01	LDO 5	INL 6	LDO 3	LDO 8	LDO 1
N	NC	LX5	INB 04	LX4	PGN D 4	PGN D 1	LX1	INB 01	LDO 7	INL 5	LDO 6	LDO 4	NC

TOP VIEW

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UME300

3. PIN CONFIGURATION

	1	2	3	4567				8	9	10	11	12	13	14
A				DNU		DNU			DNU		DNU			
B		DNU											DNU	
C														
D	DNU													DNU
E														
F														
G														
H	DNU	NC	DAT0m	DAT1m	DAT2m	NC	NC	VDDQd	VSSQd	VSSd	VDDd	VSSQd	NC	DNU
J	NC	DAT3m	DAT4m	DAT5m	DAT6m	DAT7m	NC	NC	NC	NC	NC	DQ15d	VDDQd	NC
K	VSSd	VDDIm	A4d	VSSQm	NC	VDDQm	NC	NC	NC	NC	NC	DQ14d	DQ13d	VDDQd
L	A5d	A6d	A7d	NC								DQ11d	DQ12d	VSSQd
M	A12d	A11d	A8d		NC	VDDm	VSSm	NC	NC	NC		DQ10d	DQ9d	DQ8d
N	VDDd	NC	A9d		VDDm					NC		UDQSd	UDMd	VSSQd
P	CKEd	/CSd	NC		VSSm					NC		CKd	VDDQd	VDDd
R	VDDQd	/RASd	/WEd		NC					VSSm		/CKd	VDDQd	VSSd
T	NC	/CASd	NC		NC					VDDm		LDQSd	LDMd	VSSQd
U	BA1d	VSSd	A10d		RSTm	NC	NC	VSSm	VDDm	NC		DQ5d	DQ6d	DQ7d
V	BA0d	A0d	A1d									DQ3d	DQ4d	VSSQd
W	VSSd	VDDd	A2d	VDDQm	CMDm	CLKm	NC	NC	NC	NC	NC	DQ1d	DQ2d	VDDQd
Y	NC	VSSQm	A3d	VDDQm	VSSQm	VSSQd	NC	NC	NC	NC	NC	DQ0d	VDDQd	NC
AA	DNU	NC	VDDQm	VSSQm	VDDQm	VSSQm	NC	VDDQd	VSSQd	NC	VDDd	VSSQd	NC	DNU
AB														
AC														
AD														
AE	DNU													DNU
AF														
AG		DNU											DNU	
AH				DNU		DNU			DNU		DNU			

169 FBGA: Top View (Ball Down)

	Mobile SDRAM
	moviNAND
	Power
	Ground
	NC / DNU

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U100

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	NC	PM_H	GND	PM_L	GPO3	VDD1V8_TXDCO	GND	MI1	VDDBAT	CEXT_DCXO	XO	XOX	NC	A
B	VDDBAT_TXRF	VDD_TXRF	NB	NB	GPO2	NB	NB	MI2	D2B_OUT	AFC_DAC	XO_SUP	XO_EXT	VDD1V8_SCU	B
C	PA_RF	D2B_OUT_TXRF	GND	CEXT_TXMS	VDD2V5_TXBIAS	VDD2V5_TXDCO	GND	GND	VDD1V8_DIG	GND	GND	DI3_TX_DAT	DI3_RX_DAT	C
D	PA_POW_DET	VDD1V8_FBR	SPI_CLK	SPI_DRW	VDD1V8_TXLO	NB	NB	CEXT_TXPLL	GND	VDD2V5_FSYS	NB	DI3_TX_DATX	DI3_RX_DATX	D
E	GND	RX_L1	VSPI	SPI_SS	GND	GND	GPO1	VDD1V8_TXMS	VDD_TEST	NB	NB	VDDIO	REF_CLK_EN	E
F	RX_L2	RX_L1X	VDD1V8_RCBB	GND	GND	GND	VDD1V8_RCMS	GND	VDD1V2_DIG	GND	NB	SYS_CLK_EN	SYS_CLK	F
G	RX_L2X	RX_M1	GND	GND	VDD1V8_RCLO	GND	GND	GND	GND	GND	NB	FSYS1	FSYS1_EN	G
H	RX_M2	RX_M1X	GND	GND	GND	GND	NB	NB	CEXT_RXPLL	GND	NB	FSYS2_EN	FSYS2	H
J	RX_M2X	RX_H1	GND	VDD2V5_RCBB	VDD2V5_RCRF	GND	GND	VDD2V5_RXDCO	GND	GND	GPO8	FSYS3	FSYS3_EN	J
K	RX_H2	RX_H1X	NB	NB	GND	GND	NB	NB	VDD1V8_RXPLL	GND	GPO7	RESET_N	CLK_ON	K
L	RX_H2X	VDD1V8_RCRF	GND	RD_L1	RD_L1X	RD_H	RD_HX	GND	VDD1V8_RXDCO	VDD2V5_RFC	GND	GND	VDD1V8_RFC	L
M	NC	GND	RD_L2	RD_L2X	RD_M	RD_MX	GND	GPO4	GPO5	GPO6	PA_BIAS	PA_RAMP	NC	M
	1	2	3	4	5	6	7	8	9	10	11	12	13	

Figure 2 Ball Diagram PG-WFWLB- 138- 2 (Top View)

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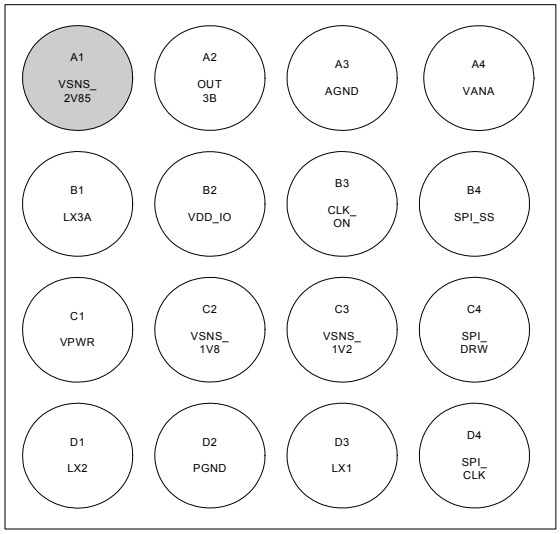
U103

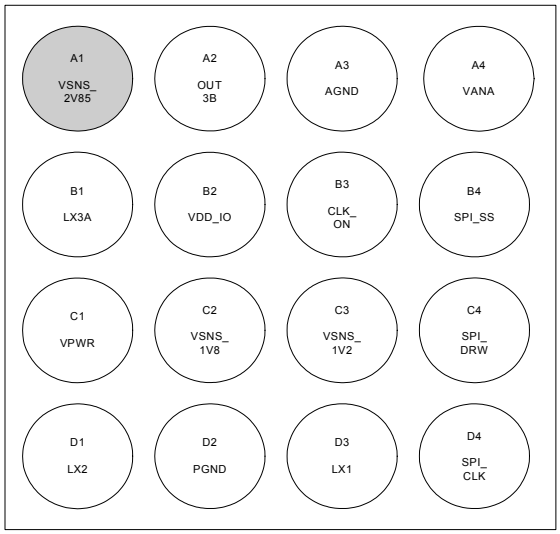
Pin Out



Bumps Down

U104

Pin Out



Bumps Down

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U708

	1	2	3	4	5	6	7
A	RSVDL	VDDQ	MHL_D	MHL_DB	NC	NC	CBUS_ID
B	RSVDL	RSVDL	RSVDL	GND	AVCC33	USB_ID	RSVDL
C	CSCL	RSVDL	WAKE_UP	AVCC12	GND	V_SENSE	INT
D	CSDA	RSVDL	GND	IOVCC18	CVCC12	CI2CA	RESET_N
E	DSDA	GND	IOVCC18	CVCC12	AVCC33	AVCC12	GND
F	RX2_P	GND	RPWR	DSCL	AVCC12	GND	HPD
G	RX2_N	RX1_P	RX1_N	RX0_P	RX0_N	RXC_P	RXC_N

Figure 2. Ball Diagram (Top View)

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U601

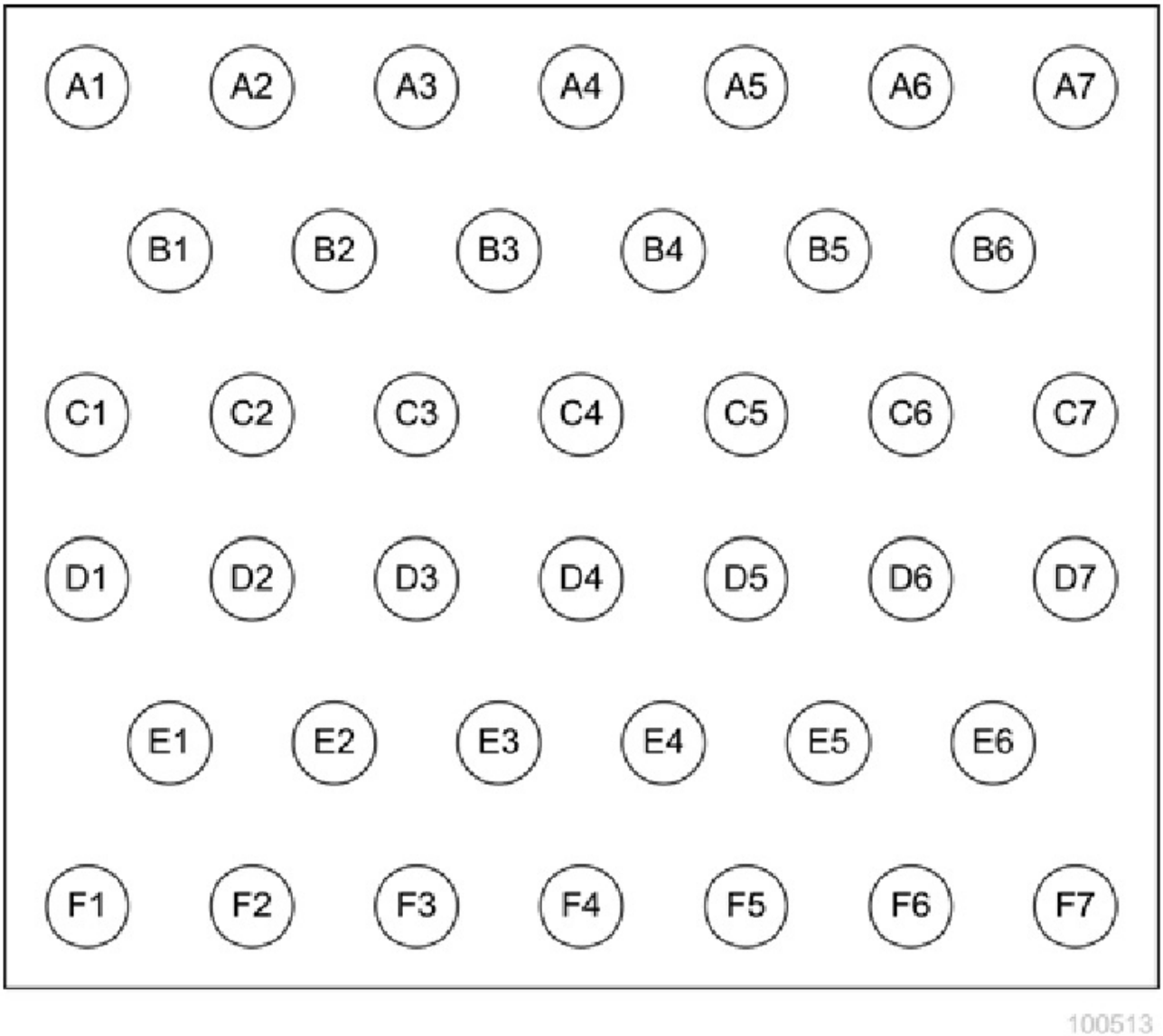

Figure 6 A1026 Ball Assignments (Top View)

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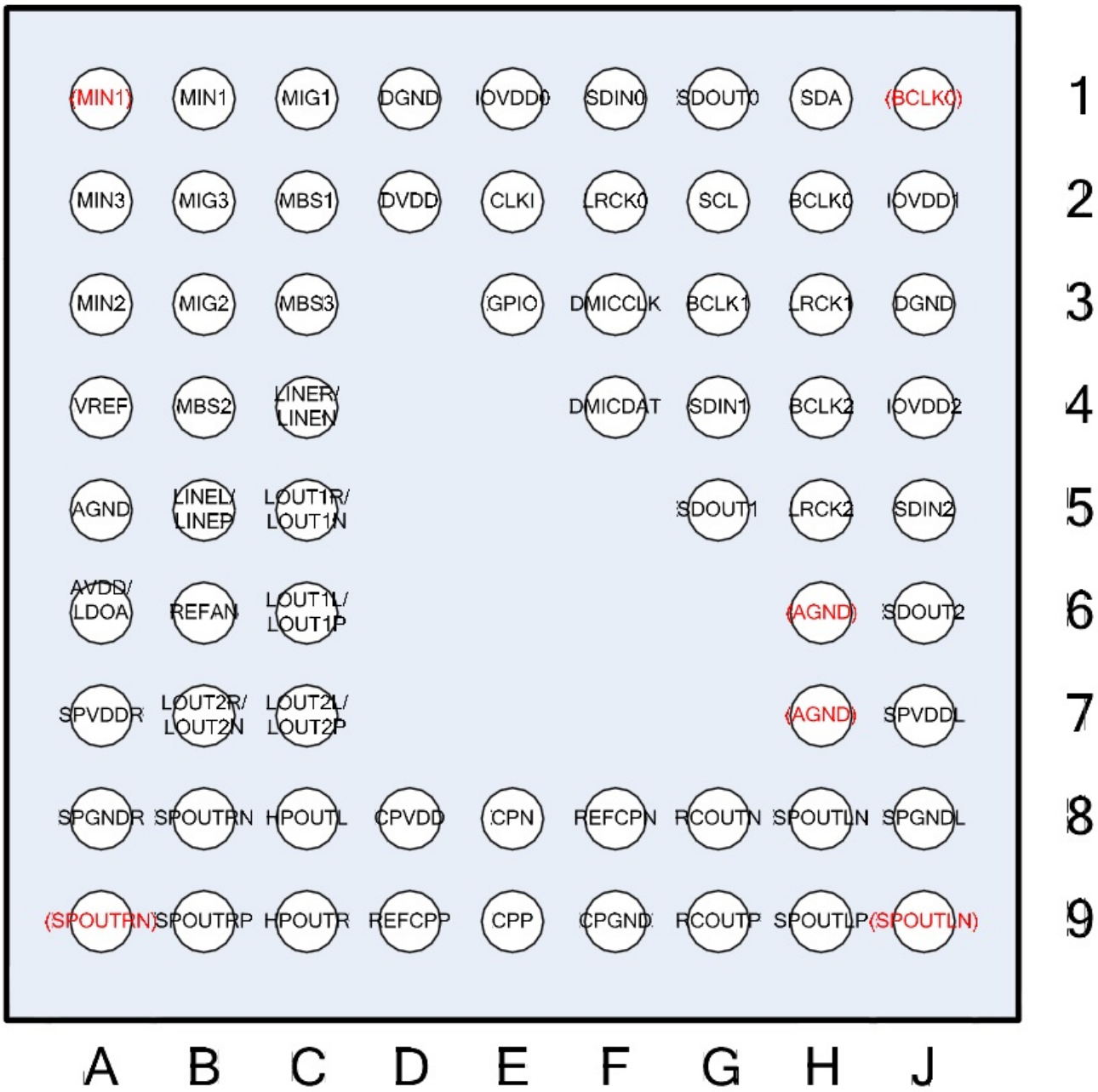
U602



67-ball WLCSP
Bottom VIEW

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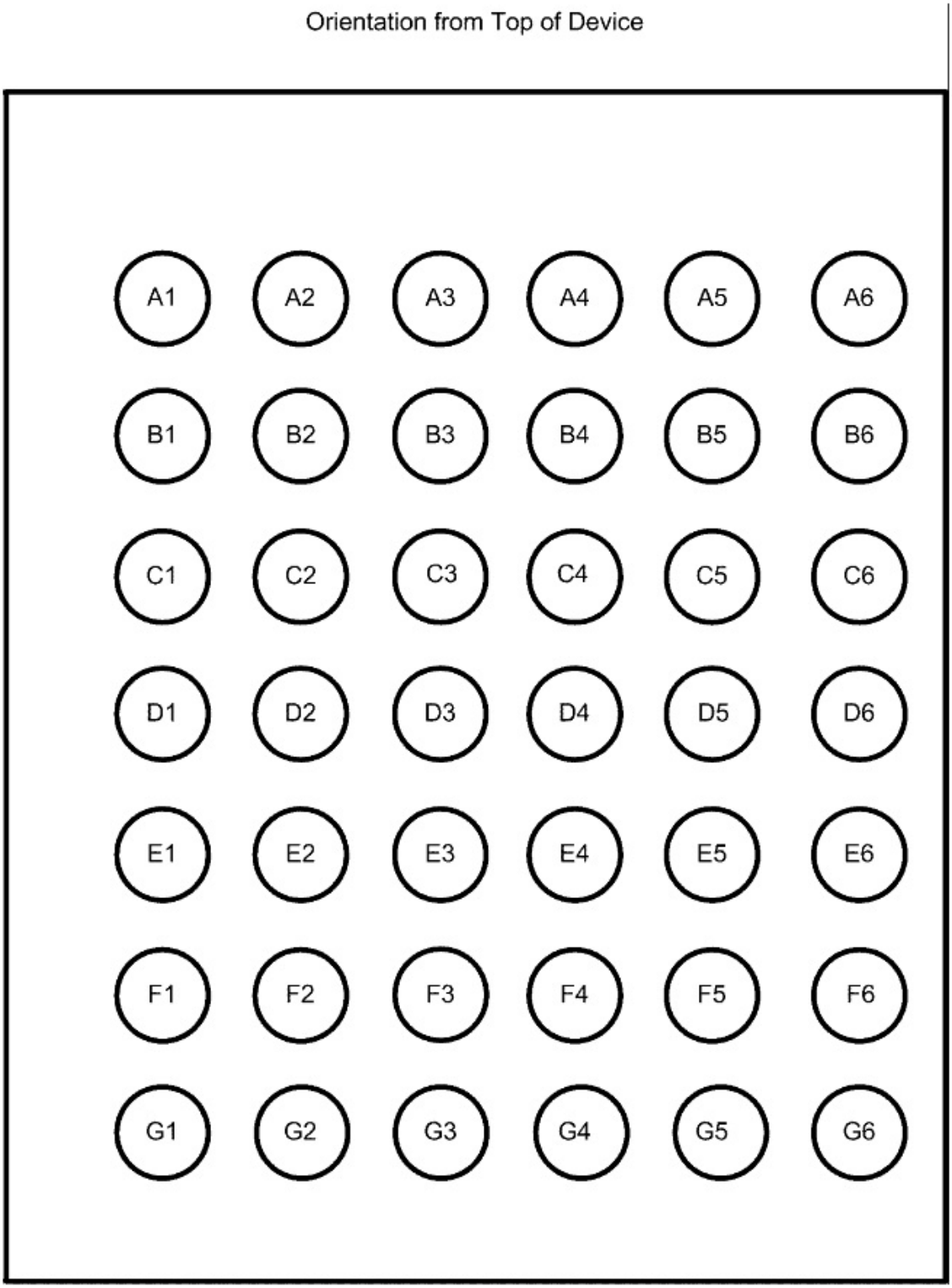
U202



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